PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-202290

(43)Date of publication of application : 30.07.1999

(51)Int.Cl. G02F 1/133
G09F 9/00

(21)Application number : 10-003700

(22)Date of filing : 12.01.1998

(71)Applicant : HITACHI LTD

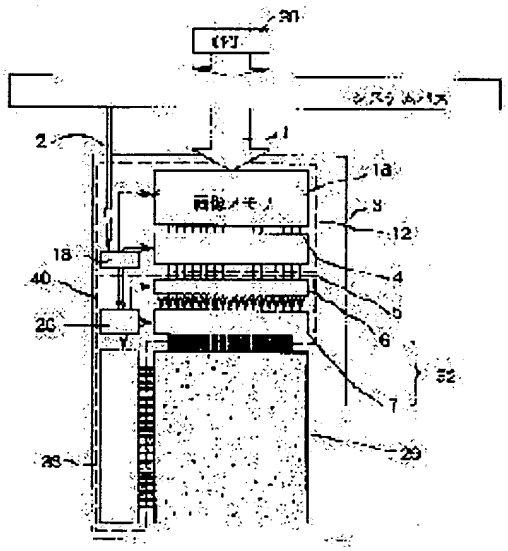
(72)Inventor : MIKAMI YOSHIAKI
KAGEYAMA HIROSHI
MASUDA KAZUTO
SATO HIDEO
KAWACHI GENSHIROU
OKUBO TATSUYA

(54) LIQUID CRYSTAL DISPLAY DEVICE AND COMPUTER SYSTEM

(57)Abstract:

PROBLEM TO BE SOLVED: To attain a power consumption reduction, miniaturization and definition improvement of a liquid crystal display with built-in peripheral circuit.

SOLUTION: The liquid crystal display device 3 provided with a liquid crystal display panel of an active matrix system forms a signal side peripheral circuit 32 and a scan side peripheral circuit 33 for driving liquid crystal and a connecting part 5 having a trunk bus for transferring display data to signal wiring on a TFT substrate. An image memory chip 12 forming an image memory 13 for storing the display data written from a CPU 30 for at least one horizontal line or a read control circuit 18 is mounted through the connecting part 5 onto the liquid crystal display device 3. The display data from the memory chip 12 are transferred from a line memory parallel interface 4 to a parallel input interface 6 for every line portion by a low-speed clock.



LEGAL STATUS

[Date of request for examination]	05.02.2001
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3436478
[Date of registration]	06.06.2003
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] It has the liquid crystal layer by which at least one side has been arranged between the substrate of a transparent pair, and this substrate. Two or more scan [one side / of said substrate] wiring, In the liquid crystal display which has the display electrode connected to two or more signal wiring, two or more thin film semiconductor components formed corresponding to the intersection of those wiring, and two or more of these semiconductor devices, and ********** in another side of said substrate The liquid crystal display characterized by coming to mount the image memory chip which forms the connection which has a junction bus for transmitting an indicative data in said signal wiring on one [said] substrate, and memorizes the indicative data for the horizontal of one line at least through said connection.
[Claim 2] It has the liquid crystal layer by which at least one side has been arranged between the substrate of a transparent pair, and this substrate. Two or more scan [one side / of said substrate] wiring, In the liquid crystal display which has the display electrode connected to two or more signal wiring, two or more thin film semiconductor components formed corresponding to the intersection of those wiring, and two or more of these semiconductor devices, and ********** in another side of said substrate On one [said] substrate, the connection which has a junction bus for transmitting an indicative data in said signal wiring is formed. The image memory chip which memorizes the indicative data for the horizontal of one line at least through said connection is mounted. Said image memory chip While carrying out address attachment of said indicative data and memorizing it to a reading horizontal direction one by one The store circuit as for which the indicative data for the horizontal of one line of the same address is read and made to coincidence, The memory output latch holding the indicative data for one line, and the latch selection circuitry which chooses said output latch's output and is connected to said junction bus, The liquid crystal display characterized by coming to constitute the read-out control circuit which controls selection connection of said latch selection circuitry while controlling to read the indicative data from said store circuit, and to latch to said memory output latch for every level Rhine one by one.
[Claim 3] It has the liquid crystal layer by which at least one side has been arranged between the substrate of a transparent pair, and this substrate. Two or more scan [one side / of said substrate] wiring, In the liquid crystal display which has the display electrode connected to two or more signal wiring, two or more thin film semiconductor components formed corresponding to the intersection of those wiring, and two or more of these semiconductor devices, and ********** in another side of said substrate On one [said] substrate, the connection which has a junction bus for transmitting an indicative data in the signal side circumference circuit for driving said liquid crystal, a scan side circumference circuit, and said signal wiring is formed. The liquid crystal display characterized by coming to mount the image memory chip which memorizes the indicative data for the horizontal of one line at least through said connection.
[Claim 4] It has the liquid crystal layer by which at least one side has been arranged between the substrate of a transparent pair, and this substrate. Two or more scan [one side / of said substrate]

wiring, In the liquid crystal display which has the display electrode connected to two or more signal wiring, two or more thin film semiconductor components formed corresponding to the intersection of those wiring, and two or more of these semiconductor devices, and ********** in another side of said substrate On one [said] substrate, the connection which has a junction bus for transmitting an indicative data in the signal side circumference circuit for driving said liquid crystal, a scan side circumference circuit, and said signal wiring is formed. The image memory chip which memorizes the indicative data for the horizontal of one line at least through said connection is mounted. Said image memory chip While carrying out address attachment of said indicative data and memorizing it to a reading horizontal direction one by one The store circuit as for which the indicative data for the horizontal of one line of the same address is read and made to coincidence, The memory output latch holding the indicative data for one line, and the latch selection circuitry which chooses said output latch's output and is connected to said junction bus, The liquid crystal display characterized by coming to constitute the read-out control circuit which controls selection connection of said latch selection circuitry while controlling to read the indicative data from said store circuit, and to latch to said memory output latch for every level Rhine one by one.

[Claim 5] A signal selection means to incorporate the indicative data for ****** level 1 Rhine for the input circuit which makes selection connection with said junction bus in said signal side circumference circuit one by one in claim 4, The level shifter which transforms into the logic electrical potential difference of said signal side circumference circuit the logic electrical potential difference of said indicative data expressed by binary data, It has the liquid crystal driver voltage generating circuit which changes an indicative data into the liquid crystal driver voltage of an analog with the Rhine latch holding the indicative data for the horizontal of one line. The liquid crystal display characterized by coming to prepare for said memory chip or said liquid crystal panel the transfer control circuit controlled to synchronize selection actuation of the both sides of said latch selection circuitry of the said signal selection means and said image memory of said signal side circumference circuit.

[Claim 6] It is the liquid crystal display characterized by performing connection and a change of a block unit when selection actuation of said signal selection means of said latch selection circuitry of said image memory and said signal side circumference circuit divides the indicative data for the horizontal of one line into two or more blocks in claim 5 and it transmits.

[Claim 7] It is the liquid crystal display characterized by constituting so that it may **** to two or more signal wiring blocks which said signal selection means of said signal side circumference circuit becomes from the same number as said junction bus about the signal wiring for said horizontal of one line in claim 5 and selection connection of this block and said junction bus may be made using a semi-conductor analog switch.

[Claim 8] It is the liquid crystal display characterized by connecting said level shifter in claims 5, 6, or 7 between said junction bus and said signal selection means or after said signal selection means.

[Claim 9] In the image memory which memorizes an indicative data, at least, it reads one by one, and address attachment of the indicative data for the horizontal of one line is carried out horizontally, and it is memorized. The store circuit which the indicative data for the horizontal of one line of the same address can coincidence read, The read-out control circuit controlled to read the indicative data memorized to the store circuit in the first half one by one, and to latch to a memory output latch for said every level Rhine, The image memory characterized by coming to provide the latch selection circuitry which makes selection connection of said memory output latch's output for said every number of fixeds number of line into a signal junction bus with the signal line of the number of fixeds number of line.

[Claim 10] In the computer system which connected CPU, memory, I/O I/O, and an indicating equipment by the system bus, said indicating equipment is mounted in the liquid crystal display panel and this panel of an active matrix, and they are new or the computer system characterized by having the image memory which the indicative data of a modification part is written in and memorizes a part for the horizontal of one line at least from said CPU.

[Claim 11] The system power which supplies drive power to each of the component in a system in claim 10, and the computing system characterized by preparing ** / power control section which carries out **

for supply of drive power according to the operating status of components other than said display.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a liquid crystal display, and relates to the liquid crystal display which mounted the image memory chip on the TFT substrate of a liquid crystal display panel.
[0002]
[Description of the Prior Art] The method which forms a matrix circumference circuit on a glass substrate, using a thin film transistor as a drive circuit of a small and high definition liquid crystal display panel is learned. For example, it is reported to 348-345 pages of "EKUSU ten dead abstract OBU 1997 International conference-on solid-state device and MATERIARUSU." Moreover, detail of a active-matrix drive method and a liquid crystal display module is given to "the liquid crystal display technique (Sangyo Tosho Publishing)" of the work edited by Shoichi Matsumoto in detail.
[0003] The configuration of the conventional TFT-liquid-crystal display module is shown in drawing 2 . In information machines and equipment, such as a personal computer, the indicative data which CPU30 or a display-control circuit becomes from the coordinate of each dot of a dot-matrix display and the combination of gradation data about a display day is generated. The image memory 13 which stores an indicative data is another arranged in the liquid crystal display 3 which really formed the display 29 and the circumference circuit section of a TFT active matrix with CPU and the display-control circuit.
[0004] In order to reduce a wiring number, serial transmission of the data from the image memory 13 to the liquid crystal display module 3 is carried out. A display-control circuit is read from an image memory 13 per several dots, and after it carries out rearrangement processing to a serial, it is sent to a liquid crystal display module as serial transmission data 8. Serial data is the serial parallel conversion circuit 9, it is again rearranged into the parallel signal of the data for one line, is changed into the signal wiring driving signal of a active matrix by the Rhine latch and the liquid crystal gradation drive circuit 10, and drives a display 29.
[0005] Between the image memory of this system, and a display-control circuit, and between a display-control circuit and a liquid crystal display module, the data for all pixels are usually transmitted at high speed by the repeat in a cycle of 60-75Hz.
[0006]
[Problem(s) to be Solved by the Invention] With the above-mentioned conventional technique, the indicative data of all pixels must be transmitted for every frame time to a liquid crystal display module. It increases, so that the number of pixels of the transfer rate at this time increases, for example, with a 1024x768-pixel configuration, a transfer with a high speed of about 50MHz is needed. For this fast transfer, LSI in a module must operate at this rate. Since a CMOS circuit is used, as for the basic circuit built in LSI, power consumption increases with a working speed. For this reason, definition followed the liquid crystal module of this method on becoming large, and it had the problem said that power consumption increases.
[0007] Moreover, the TFT circumference circuit technique which constitutes the circumference circuit of the liquid crystal display section is used with the small display. However, compared with the circuit

of LSI formed on Si chip, since the polycrystal thin film Si and the vacuum evaporationo film SiO2 are used as gate dielectric film, mobility is low and a circuit working speed is also slow. For this reason, highly-minute-izing by the conventional TFT circumference circuit was difficult.

[0008] The purpose of this invention is to offer the liquid crystal display which the data transfer frequency from an image memory to a liquid crystal module can fall sharply, and can reduce clock frequency and power consumption in view of the trouble of the conventional technique, and can be miniaturized.

[0009] Moreover, the liquid crystal display which mounted the image memory is connected, and it is in offering the computing system which can improve reduction of power consumption, and the processability of CPU.

[0010] Furthermore, the indicative data for level 1 Rhine is memorized at least, and it is in offering the possible image memory of division read-out corresponding to the number of output signal lines.

[0011]

[Means for Solving the Problem] This invention for attaining the above-mentioned purpose The substrate of a pair at least with transparent one side, It has the liquid crystal layer arranged between this substrate. Two or more scan [one side / of said substrate] wiring, In the liquid crystal display which has the display electrode connected to two or more signal wiring, two or more thin film semiconductor components formed corresponding to the intersection of those wiring, and two or more of these semiconductor devices, and ********** in another side of said substrate On one [said] substrate, the connection which has a junction bus for transmitting an indicative data in said signal wiring is formed, and it is characterized by coming to mount the image memory chip which memorizes the indicative data for the horizontal of one line at least through said connection.

[0012] Moreover, the signal side circumference circuit for driving said liquid crystal and a scan side circumference circuit are formed on the TFT substrate which constitutes said liquid crystal panel, and it is characterized by coming to connect the input and said junction bus of said signal side circumference circuit.

[0013] Moreover, while said image memory chip carries out address attachment of said indicative data and memorizes it to a reading horizontal direction one by one The store circuit as for which the indicative data for the horizontal of one line of the same address is read and made to coincidence, The memory output latch holding the indicative data for one line, and the latch selection circuitry which chooses said output latch's output and is connected to said junction bus, While controlling to read the indicative data from said store circuit, and to latch to said memory output latch for every level Rhine one by one, it is characterized by coming to constitute the read-out control circuit which controls selection connection of said latch selection circuitry on semi-conductors, such as a silicon chip.

[0014] Since according to the description of this image memory chip it outputs to the signal junction bus with the signal line of the number of fixeds number of line of arbitration alternatively and the indicative data for one line can be transmitted to it, it is effective also as general-purpose image memory.

[0015] Moreover, a signal selection means to incorporate the indicative data for ****** level 1 Rhine for the input circuit which makes selection connection with said junction bus in said signal side circumference circuit one by one (for example, block electronic switch), The level shifter which transforms into the logic electrical potential difference of said signal side circumference circuit the logic electrical potential difference of said indicative data expressed by binary data, It has the liquid crystal driver voltage generating circuit which changes an indicative data into the liquid crystal driver voltage of an analog with the Rhine latch holding the indicative data for the horizontal of one line. It comes to prepare for said memory chip or said liquid crystal panel the transfer control circuit controlled to synchronize selection actuation of the both sides of said latch selection circuitry of the said signal selection means and said image memory of said signal side circumference circuit.

[0016] Moreover, selection actuation of said signal selection means of said latch selection circuitry of said image memory and said signal side circumference circuit is characterized by performing connection and a change of a block unit, when dividing and transmitting the indicative data for the horizontal of one line to two or more blocks.

[0017] Or said signal selection means of said signal side circumference circuit **** signal wiring for said horizontal of one line to two or more signal wiring blocks which consist of the same number as said junction bus, and is characterized by constituting so that selection connection of this block and said junction bus may be made using a semi-conductor analog switch.
[0018] Moreover, said level shifter is characterized by connecting between said junction bus and said signal selection means or after said signal selection means.
[0019] According to this invention, the image memory was mounted on the liquid crystal panel in which the display and TFT circumference circuit of a TFT active matrix were formed, and parallel connection of an image memory and a circumference circuit is realized on a substrate. For this reason, since an indicative data is always held at an indicating-equipment side, rewriting of an indicative data requires only a modification part, and the transfer frequency from CPU to an indicating equipment can reduce it sharply. Moreover, since it becomes the parallel transfer of the horizontal of one line at the maximum, a transfer frequency falls, and the data transfer from an image memory to a circumference circuit can reduce the clock frequency and power consumption of the whole display sharply.
[0020] In the computer system to which this invention which attains the purpose besides the above connected CPU, memory, I/O I/O, and an indicating equipment by the system bus, said indicating equipment is mounted in the liquid crystal display panel and this panel of an active matrix, and from said CPU, the indicative data of a modification part is written in and it is characterized by new or having the image memory which memorizes a part for the horizontal of one line at least.
[0021] Moreover, it is characterized by preparing ** / power control section which carries out ** for supply of drive power according to the operating status of the system power which supplies drive power, and components other than said display in each of the component in a system.
[0022] The basic configuration of the liquid crystal display by this invention is shown in drawing 1 . The indicative data and control signal from CPU30 are transmitted to a display 3 through the data address bus 1 and the control signal line 2. The indicating equipment 3 mounts the image memory chip 12 in the connection 5 which formed the TFT circumference circuit 40 which used the display 29 of a TFT active matrix, and Polycrystal TFT on the TFT substrate, and was formed on the TFT substrate.
[0023] The indicative data transmitted from CPU30 is written in the image memory 13 built in the image memory chip 12. A change of the contents of a display is made by rewriting the data of the part corresponding to a modification pixel from CPU30.
[0024] The read-out control circuit 18 reads the indicative data of an image memory 13 collectively for every one line of a matrix, transmits it to the Rhine memory parallel interface 4, processes rearrangement suitably and transmits it to the TFT circumference circuit 40 with a control signal through the connection 19 including the junction bus for two or more pixels. Processing of rearrangement is needed, when 1 time of the number of parallel transfers divides one line into multiple times and performs it.
[0025] The transfer control circuit 26 controls actuation of the TFT circumference circuit section 40. First, the indicative data sent from the image memory chip 12 side is rearranged with the parallel input interface 6, and is changed into the signal wiring driver voltage of a active matrix by the liquid crystal gradation drive circuit 7. This parallel input interface 6 and the liquid crystal gradation drive circuit 7 are equivalent to the signal side circumference circuit 32. Synchronizing with the scan signal from the scan side circumference circuit 33, signal wiring driver voltage is impressed to a display 29, and the liquid crystal of a picture element part is driven.
[0026] Thus, an image memory chip is carried on the substrate which forms a liquid crystal display panel, connection of the number of multipoints of high density is made between a chip and a substrate, and parallel transmission of the data of all pixels is periodically carried out between an image memory and a TFT circumference circuit. Therefore, the clock frequency of a display can decrease sharply and low-power-ization can be attained.
[0027] Moreover, since CPU should transmit only the pixel data which change the contents of a display to a display, write-in processing of CPU can decrease sharply and expansion of the processability of CPU and reduction of power consumption are attained. This description has a large merit at small

machines, such as a notebook computer.
[0028] Moreover, by reduction of the clock frequency of the drive circuit of a display, a high definition display is attained also by the circumference circuit on a TFT substrate with actuation slower than Si chip, modular mounting components mark are reduced, and it can miniaturize.
[0029]
[Embodiment of the Invention] Hereafter, two or more examples of the liquid crystal display of this invention are explained to a detail, referring to a drawing. In addition, the same sign is given to the equivalent element through each drawing.
[0030] [Example 1] The liquid crystal display structure of a system of an example 1 is shown in drawing 3 . The liquid crystal display of this example consists of image memory chips 12 mounted in the connection 5 formed on the same TFT substrate as the liquid crystal display panel 11 which consists of a display 29 with the pixel of the active matrix formed on the TFT substrate, and its TFT circumference circuit.
[0031] The liquid crystal display panel 11 is based on the configuration on the conventional TFT substrate. A transistor component is formed in the intersection of the two or more scan wiring and signal wiring which intersect perpendicularly mutually. The display 29 which **** liquid crystal with the display electrode and counterelectrode which were connected to the gate electrode and drain electrode of this component, forms a pixel, and comes to arrange this pixel to the above-mentioned intersection in the shape of a matrix, Since the pixel of an active matrix is driven, it consists of a scan side circumference circuit 33 which supplies the signal side circumference circuit 32 and scan signal which supply a status signal. The signal side circumference circuit 32 is different from the conventional configuration so that it may mention later.
[0032] The junction bus 19 of a connection 5 etc. is formed on a TFT substrate of a CMOSTFT formation process, connects the outgoing end of the image memory chip 12, and the input edge of the signal side circumference circuit 32, and makes the parallel transmission of a status signal possible.
[0033] While the image memory chip 12 is formed on Si chip, reading the indicative data for one frame one by one in a part for the horizontal of one line, and this example at least, carrying out address attachment horizontally and memorizing The image memory 13 memorized possible [coincidence read-out of the indicative data for one line of the same address], The indicative data of an image memory 13 is read one by one with the memory output latch 16 holding the indicative data for one line. The read-out control circuit 18 controlled to latch the read indicative data to the memory output latch 16 for every level Rhine one by one and the latch selection circuitry 17 which makes selection connection of latch's 16 output into the junction bus 19 are provided.
[0034] Moreover, the transfer control circuit 26 controlled by the both sides of the latch selection circuitry 17 and the signal side circumference circuit 32 of the liquid crystal display panel 11 to synchronize selection actuation is formed. In addition, the transfer control circuit 26 is not the image memory chip 12, and may be established in the liquid crystal display panel 11 side.
[0035] The cross-section structure of the outline of a liquid crystal display is shown in drawing 4 . The liquid crystal display panel 11 seals liquid crystal 43 with the liquid crystal seal 44 among these, puts it with two polarizing plates 45 from those outsides, and comes to combine a back light 46 with the TFT substrate 41 which forms TFT, and the opposite substrate (glass substrate) 42 in which the transparence electric conduction film 49 containing a color filter 48 and tin oxide was formed on the front face. The transistor component from which the display 29 only illustrating a part serves as a drive circuit at the substrate 41 of the liquid crystal 43 bottom is formed in the shape of a matrix. The circumference circuit 40 of a display 29 is formed in the substrate 41 of the outside of the field which is pinching liquid crystal 43.
[0036] Furthermore, on the TFT substrate 41 of the outside between polarizing plates 45, the image memory chip 12 is mounted and the junction bus 19 which connects the circumference circuit 40 with a chip 12 is formed. It connects with the chip input terminal 37 through wiring on the TFT substrate 41 etc., and the image memory chip 12 is connected with the bus wiring 38 using a flexible printed circuit board etc.

[0037] Alkali free glass is used for a TFT substrate as Si film, and the low-temperature polish recon by the laser annealing grown method is used for formation of a TFT substrate as the Si crystal film formation approach. Or polycrystal Si film, such as elevated-temperature polish recon by the solid phase grown method, is used using a quartz-glass substrate. The doping method is combined with this and TFT of pchnch is formed on the same substrate at coincidence.
[0038] The conventional LSI process can constitute the image memory chip 12 with a connection part with the TFT substrate 41. Moreover, connection by ** pitch wiring of 100 micrometers or less is possible for the connection with the bus wiring 38, and the image memory chip 12 and the TFT substrate 41 by using ANISORUMU which is the goods of the anisotropy electric conduction film of Hitachi Chemical Co., Ltd.
[0039] Next, the configuration and actuation of the liquid crystal display of this example are explained to a detail according to drawing 3 . Through the address bus wiring 34 and the data bus wiring 35, the indicative data changed into the pixel address and the gradation data for every pixel is inputted into the memory chip 12 of an indicating equipment 3 by CPU30 with the control signal for the data transfer timing control by the control signal line 36, and is written in an image memory 13 through the data-line decoder 14, the word line decoder 15, and the data interface circuit 50.
[0040] In addition, conversion to the gradation data for every dot is good also by logical devices which assign the memory area according to individual every [1 dot of a display, or] two or more dots, such as a display controller which has the function to generate an indicative data and the address in a bit map addressing format.
[0041] The indicative data memorized in the image memory 13 controls word line DEKOTA 15 from the read-out control circuit 18, only several display data bit minutes for the horizontal of one line of an image memory 13, carries out a sequential sampling and reads it to the memory output latch 16. The indicative data for one line latched to the memory output latch 16 is divided into two or more blocks, is chosen at a time in predetermined sequence by 1 block of latch selection circuitries 17, and is outputted from the chip output connection terminal 31 with the number for 1 block.
[0042] The indicative data outputted in the block unit is inputted into the signal side circumference circuit 32 of the liquid crystal display panel 11 on the same substrate through the junction bus 19 formed on the TFT substrate from a memory chip 12. Actuation of the signal side circumference circuit 32 is controlled by the transfer control circuit 26.
[0043] First, the block electronic switch 20 outputs the data of a block unit for every block chosen from the selection latch circuit 21. The logic signal level of an indicative data is changed into the logic electrical potential difference of a TFT circumference circuit by the level shifter 22 at this time. When the indicative data for one line is held by transmitting every block one by one at the selection latch circuit 21, it is transmitted to the Rhine latch 23 all at once.
[0044] The liquid crystal driver voltage generating circuit 24 changes an indicative data into a liquid crystal gradation electrical potential difference, and drives the drain wiring 106 of a display 29. On the other hand, the gate wiring 110 of a display 29 is driven by the gate wiring drive circuit 27 and the scan side circumference circuit 33 which consists of a scan shift register 28. The shift clock 113 and the frame start signal 114 used as scan timing are supplied from the transfer control circuit 26. The above transfer operation of one line is carried out by all Rhine to an one-frame within a time, and the display of one screen is realized.
[0045] In the above-mentioned configuration, the number of data of 1 block increases, so that there are many bus numbers of the junction bus 19, and the count of a data transfer can be decreased. Although it depends for a bus number on the precision of processing equipment, since it becomes connectable [50 micrometer pitch] with the chip of 5mm angle in the present equipment, the ejection of 300 terminal extent becomes possible by using 100 terminals and three sides per side. Since terminal formation of about further 3 times is possible by using a terminal configuration as an alternate pattern, the connection whose 1 block is about 300 bits is easy.
[0046] The example of application of the liquid crystal panel of practical use is explained. By the 640x480-pixel panel, to transmit 640 pixels for one line, and a gradation signal with a color [RGB

each] of 6 bits, it is necessary to transmit 640x3x6=11520 bit. Therefore, the count of a transfer in the case of a 300-bit parallel transfer becomes 38.4 times. Since the period of one line is set to 1/70/480=29.8microsecond by the transfer time in the case of 70Hz frame frequency, the transfer frequency in this case is set to 1.3MHz. Since the dot clock of the conventional example is set to 20MHz or more, it turns out that it becomes sharp frequency reduction. Moreover, much more reduction is possible by dividing an image memory chip into plurality, synchronizing it with it, and driving.

[0047] The detailed configuration and actuation of each circuit are explained. The configuration of an image memory chip is shown in drawing 5 . The image memory chip 12 is connected with a system bus through the address bus wiring 34, the data bus wiring 35, the bus wiring 38 into which the control signal line 36 was packed, and the chip input connection terminal 37.

[0048] The word line 62 to arrange a memory cell 63 in the shape of a matrix, and for an image memory 13 choose each memory cell is connected to word line DEKOTA 15 common to a line writing direction. The bit line 65 which writes in data is connected to the bit line drive circuit 51 common to the direction of a train. The bit line drive circuit 51 is written in and consists of the data interface 50 and data-line DEKOTA for control. It connects with a sense amplifier 64, the cel for one line which corresponds if a word line is chosen is chosen, and each of a bit line 65 outputs the condition of a cel to a sense amplifier 64 all at once.

[0049] The condition of a bit line 65 is changed into data by the sense amplifier 64, and it is read to the memory output latch 16 by the memory latch control signal 131, and connects with the latch selection circuitry 17. It connects with two or more chip output terminals 31, and the output of the latch selection circuitry 17 is connected with a liquid crystal panel 11 through the junction bus 19.

[0050] Among these, the bit line drive circuit 51 for writing in a memory cell 63 and word line DEKOTA 15 are the same as that of the method of a dual port memory chip, and good.

[0051] The control signal for controlling the write-in actuation to memory 13 is generated by the read-out control circuit 18, and is supplied to word line DEKOTA 15 and the bit line drive circuit 51. Moreover, the memory latch control signal 131, the memory chip block change signal 130, and the control signal of the transfer control circuit 26 which controls actuation of a TFT circumference circuit are also generated. The transfer control circuit 26 outputs the block selection signal 84, the block latch signal 88, the Rhine latch signal 132, the shift clock 113, and the frame start signal 114. In addition, the control signal to a TFT circumference circuit has added and transmitted the number required for the junction bus 19.

[0052] The circuitry of a memory cell is shown in drawing 6 . The memory cell 63 was constituted by six transistors and has connected the VDD terminal 66 and the VSS terminal 67 to a power source. The bit terminal 69 and the reversal bit terminal 70 which output and input a reversal signal mutually [in order to output and input the WORD terminal 68 for choosing a cel and data] are connected to the word line 62 of a matrix, and a bit line 65, respectively.

[0053] The circuitry of a sense amplifier is shown in drawing 7 . If a sense amplifier 64 is constituted by five transistors and a power source VDD and bias voltage VCS are impressed, it will impress the bit signal and reversal bit signal which are reversed mutually to an input terminal 71, and will obtain the data output 72 which has the amplitude of supply voltage.

[0054] Memory output latch's circuitry is shown in drawing 8 . The input edge is connected to the data output terminal 72 of a sense amplifier 64, and two or more latch circuits 97 arranged at juxtaposition are latched all at once with the memory latch control signal 131.

[0055] The configuration of a latch circuit is shown in drawing 9 . A latch circuit 97 consists of two inverters 90 with a CMOS transistor, and the two transfer gates 91 and the control inverters 92. Only when the memory latch control signal 131 inputted into the control terminal 94 from the read-out control circuit 18 is logic "forward", the transfer gate 91 serves as open, and the data from the sense amplifier 64 inputted into the input terminal 93 drive an inverter 92, and change the condition of the latch output 95. When the memory latch control signal 131 is logic "negative", an output state does not change but holds data.

[0056] The configuration of a latch selection circuitry is shown in drawing 10 . The latch selection

circuitry 17 makes sequential connection of the data line 134 for one line of the total N bit from the memory output latch 16 into m output buses 82 through the analog switch 135 which used the transfer gate. For this reason, the data line is divided every m, it considers as the output block 81 of block 1 - h, and selection connection is multiplexed and made for every output block. Since the data line of N book is divided into h blocks corresponding to m output buses, it becomes the relation of block count h=N/m.
[0057] The block 81 which connects with the output bus 82 and is outputted is performed by control of an analog switch 135. For this reason, only a specific output block is alternatively connected by packing a selection-signal input terminal by using an analog switch 135 as the block analog switch 83 for every block, impressing a logic "forward" signal only to any that one, and impressing a logic "negative" signal to others. The memory chip block change signal 130 is supplied from the read-out control circuit 18, and since the control signal which the polarity reversed for control of an analog switch is the need, an inverter 85 is connected every change signal 130. The output bus 82 is connected to the junction bus 19 through the chip output connection terminal 31.
[0058] Next, the configuration and actuation of the signal side circumference circuit 32 and the scan side circumference circuit 33 are especially explained to a detail about the liquid crystal panel of this example.
[0059] The block electronic switch 20 of the signal side circumference circuit 32 transmits the indicative data inputted through the junction bus 19 from the image memory chip 12 in order of a block, and the selection latch circuit 21 carries out the rearrangement of the indicative data for one line.
[0060] The configuration of a block electronic switch is shown in drawing 11 . The output wiring 136 for one line (N book) of the block electronic switch 20 is divided into 1-h blocks, and is connected to the junction bus 19 through the TFT analog switch 161 and the input bus 86 for 1 block (m) which are constituted by CMOSTFT.
[0061] An analog switch is packed every m pieces and constitutes the TFT block analog switch 160. The control signal of a switch 160 generates the control signal of amphipathy required for analog switch control with an inverter 89 in common for every block. By impressing a logic "forward" signal only to any one, and impressing a logic "negative" signal to others with the block selection signal 84 supplied from the transfer control circuit 26, each block is chosen in predetermined order and closing motion of a switch is connected with the input bus 86. The indicative data expressed by the output wiring 136 of the block output 87 connected with the input bus 86 fits the logical level of the output signal of an image memory 13 to the logical level of a thin film transistor circuit by the level shifter 22, and is sent to the selection latch circuit 21.
[0062] The circuitry of a selection latch and the Rhine latch is shown in drawing 12 . This drawing (a) is the selection latch circuit 21, it arranges two or more latch circuits 97, packs a latch control signal for every block which consists of m, and is constituted possible [the latch of a block unit]. With the block latch signal 88 from the transfer control circuit 26, the data of the same block are latched synchronizing with the block electronic switch 20. The output of the selection latch circuit 21 is connected to the Rhine latch circuit 23. This drawing (b) is a latch circuit 97, and is constituted by CMOSTFT. However, since it becomes the same configuration as the latch circuit of drawing 9 , the sign of a circuit element supposes for convenience that it is the same.
[0063] Drawing 12 (c) is the Rhine latch 23, and is carrying out parallel connection of the same latch circuit 97 as drawing 12 (b) by N bit. Package connection is made and the latch control signal edges 94 of all the circuits 97 sample the indicative data for one line all at once with the Rhine latch signal 132 from the transfer control circuit 26.
[0064] The circuitry of a level shifter is shown in drawing 13 . A level shifter 22 consists of six transistors. The input signal from the block electronic switch 20 is inputted into the reversal signal and four transistor circuits in all by the inverter 90, and the logic electrical potential difference is amplified to the electrical potential difference of a power supply terminal 99.
[0065] Thus, a level shifter 22 is connected behind the block electronic switch 20, and the logical level of the output signal of an image memory 13 is fitted to the logical level of a TFT circuit. Consequently, power consumption can be reduced for the following reasons.

[0066] As for the block electronic switch 20, the output wiring 136 of m junction buses 19 and N book constitutes ** / matrix by which ** is carried out from an analog switch, and crossover capacity is formed in this wiring intersection. In order to change a signal to a high speed by the matrix, it is necessary to see from the image memory chip 12 and to carry out the charge and discharge of the crossover capacity to a high speed. The power consumption at this time is proportional to capacity value, and proportional to the square of signal amplitude. Then, power consumption can be reduced by lowering the driver voltage of the block electronic switch 20.
[0067] In this example, the image memory chip 12 is what was formed by LSI on a silicon substrate as a semiconductor device, and is used less than [logic electrical-potential-difference 5V] for high integration. On the other hand, operating voltage of the TFT circuit of a liquid crystal panel 11 must be made higher than liquid crystal driver voltage, and about 8-16V is specifically needed. Then, up to the block electronic switch 20, a logic electrical potential difference drives on the logic electrical potential difference of 3.3-5v, and an image memory, carries out the pressure up of the logic electrical potential difference to 10-12V by the subsequent level shifter 22, and enables the liquid crystal drive. Consequently, reduction and high-speed operation of power consumption are made possible.
[0068] In this example, since the switch change method is used for the block electronic switch 20, regardless of the logic electrical potential difference of an indicative data, the change of a signal is possible. In addition, the change of a signal is possible also by the combination of two or more logical circuits. In that case, it is necessary to carry out a level shift to the logic electrical potential difference for high-speed logical circuits constituted from the input section of the block electronic switch 20 by TFT.
[0069] The configuration of a liquid crystal driver voltage generating circuit is shown in drawing 14 . a input terminals 100 into which an a-bit digital gradation signal is inputted with a binary number are connected to the gradation voltage selection switch 104 using the transfer gate 103 through the DEKOTA circuit 101 which combined the logical circuit, and the liquid crystal driver voltage generating circuit 24 is connected with the drain wire the output line 106 of whose is the signal wiring of a display 29. The gradation voltage selection switch 104 is connected to the gradation electrical-potential-difference bus 105 which consists of wiring of a Norimoto of 2, and each wiring of a bus 105 is connected to the gradation power source 47 of different amplitude corresponding to gradation.
[0070] Therefore, the a-bit digital gradation signal connected to the input terminal 100 expresses the gradation data corresponding to the gradation number of a binary number notation. one gradation control signal corresponding to the gradation number of a binary number notation by the DEKOTA circuit 101 -- a Norimoto of 2 -- it chooses from a number of gradation control signal 102. By making it flow only through the one transfer gate 103 of the gradation voltage selection switch 104, a gradation control signal connects 1 and the output line 106 of the gradation electrical-potential-difference bus 105 to which the specific gradation power source was connected, and outputs a gradation electrical potential difference. Thereby, corresponding to the a-bit indicative data showing 1-pixel gradation, it is changed into the liquid crystal driver voltage to which the permeability of liquid crystal is changed, and is outputted to the drain wire of a picture element part from an output line 106.
[0071] Next, the scan side circumference circuit 33 of drawing 15 explains the configuration of a shift register 28 and the gate wiring drive circuit 27. A shift register 28 connects the multistage shift register circuit 112 to a serial, and the shift clock 113 of the frame start signal 114 and amphipathy is supplied to an input from the transfer control circuit 26. The gate drive circuit 27 is constituted by the inverter train 111 which carried out the series connection of the inverter one by one with big gate width, inputs the output of each stage of a shift register 28, and drives gate wiring of a display 29 at a high speed.
[0072] The circuit diagram of a shift register is shown in drawing 16 . A shift register 28 connects to a serial many shift registers 112 which consist of eight inverters 107 and the eight transfer gates 108, and is constituted. By driving with the shift clock 113 with which polarities differ mutually [two phases], it is delayed for every sequential shift clock, and an input signal 109 is outputted to the gate wiring 110.
[0073] Besides above, the read-out control circuit 18 and the transfer control circuit 26 which generate various kinds of above-mentioned control signals are constituted by the combination of the logical

circuit which used CMOS, respectively. It is the conventional technique fundamentally and detailed explanation is omitted.

[0074] Next, actuation of the liquid crystal display of this example is explained. Drawing 17 is a timing diagram which shows the write-in actuation to an image memory from CPU. As mentioned above, the address and data are specified from CPU30, and the memory select signal and the read-out control signal are included in the control signal.

[0075] If a memory select signal becomes logic "0", an image memory will be chosen and the writing to an image memory 13 will be attained. Then, the condition of a data bus in case a write-in control signal changes from logic "0" to logic "1" is written in the memory cell 63 of the appointed address of an image memory. Thus, the writing of the indicative data to an image memory 13 is performed by the same procedure as other memory connected to CPU, and does not have the conventional personal computer carrying a liquid crystal display, etc. and the changing place.

[0076] Next, read-out of an indicative data is explained. Drawing 18 is a timing diagram which shows the read-out actuation of one frame to the memory output latch from an image memory. If word line DEKOTA 15 operates with directions of the read-out control circuit 18 and it chooses 1 of a word line 62 - one n at a time one by one, a part for the data of one line of the memory cell 63 connected to the word line 62 will be inputted into a sense amplifier 64 through a bit line 65, and will be changed into digital data. If this is inputted into the memory output latch 16 one by one and is latched with the memory latch control signal 131, the output latch's 16 output will change. The above read-out actuation is repeated to 1 frame time from the 1st line to the n-th line of the scanning-line number of one screen, and a series of actuation is further repeated for every frame time.

[0077] Drawing 19 is the explanatory view showing actuation of a latch selection circuitry. The latch selection circuitry 17 outputs the memory output latch's 16 output for one line to m chip output terminals 31. A part for an indicative-data hxm bit for the horizontal of one line of scanning-line k Motome is held like the array of the illustration to the memory output latch 16. This is divided into m bits and h blocks, and it chooses in order from the 1st block to h blocks with the memory chip block change signal 130 supplied from the read-out control circuit 18. Thereby, it can connect with the output bus 82 one by one to block 1-h, and the indicative data for one line is outputted to the chip output terminal 31 and a pan per block to the junction bus 19.

[0078] Drawing 20 is the explanatory view showing actuation of the selection latch circuit which incorporates an indicative data through a block electronic switch. The data from the sequential block 1 to Block h are outputted to the junction bus 19. If the block selection signal 84 is supplied to the block electronic switch 20 from the transfer control circuit 26, the block latch signal 88 is supplied to the selection latch circuit 21 and the selection signal and block latch signal of an applicable block are made into logic "forward" synchronizing with this, data will be incorporated by the selection latch circuit 21 to which the selection block was connected, and the output will be rewritten. In this case, it is changed into the level of an about [10-12v] TFT logical circuit by the level shifter 22 connected to the input side of each selection latch circuit 21.

[0079] Thus, after renewal of sequential of the data arrangement on a selection latch is partially carried out like illustration and rewriting to 1-h blocks finishes, the data of the k-th line are arranged on a selection latch. In addition, since read-out actuation of the image memory chip 12 and actuation of the block electronic switch 20 and the selection latch circuit 21 are performed synchronously, the indicative data of one line on the memory output latch 16 of an image memory 13 is transmitted to the selection latch circuit 21 within 1 horizontal-scanning period.

[0080] Drawing 21 is a timing diagram which shows actuation of the Rhine latch. The data of scanning-line 1 duty are updated and supplied to the Rhine latch's 23 input for every 1 level period from the selection latch 21. This input data is incorporated with the Rhine latch control signal 132 from the transfer control circuit 26, and the Rhine latch output data are updated. It connects with the liquid crystal driver voltage generating circuit 24, and the Rhine latch output is changed into liquid crystal driver voltage in an instant, and is supplied to drain wiring of a correspondence pixel from an output line 106.

[0081] Actuation of a display 29 is the same as usual. The scan pulse to which each picture element part

by which the matrix configuration of the display 29 is carried out carried out the sequential shift of the pixel of 1 level Rhine from the gate wiring 110 is impressed from a scan side circuit. Moreover, in a signal side circuit, synchronizing with a scan pulse, the liquid crystal driver voltage for one line is impressed from drain wiring of each pixel from the liquid crystal driver voltage generating circuit 24, and the pixel display of the horizontal of one line is performed.

[0082] As mentioned above, according to the liquid crystal display of this example, the image memory chip mounted on the display panel memorizes the indicative data from drawing control circuits, such as CPU, by the bitmapped image, reads the digital indicative data for one line to coincidence, takes a synchronization by the transfer control circuit, and carries out a sequential output into a junction bus for every two or more pixels of a block unit. This indicative data is supplied to the circumference drive circuit which used the thin film TFT and was formed with the display on the display panel through a junction bus. A circumference drive circuit takes a synchronization by the transfer control circuit, incorporates an indicative data one by one to the selection latch for one line, transmits it to the Rhine latch, and holds the data for one line. It changes into the gradation electrical potential difference which impresses the digital gradation data of each dot to the liquid crystal of a pixel using this data.

[0083] Consequently, the interface of an image memory and a display can be simplified, and since the transfer clock for transmitting the data which are one line can be reduced, the power consumption of a display can be reduced sharply. Moreover, a liquid crystal module can be miniaturized by formation of the circumference circuit on a TFT substrate, and a high definition image can be offered.

[0084] [Example 2] Next, the 2nd example of this invention is explained. Drawing 22 is the block diagram of the liquid crystal display by the example 2. The point which is different from an example 1 is a part of signal side circumference circuit of a liquid crystal panel 11. Specifically, each terminal of the junction bus 19 is connected to the signal input selection circuitry 121 constituted from a shift register train through the level shifter 120.

[0085] The block diagram from the junction bus to the Rhine latch is shown in drawing 23 . A level shifter 120 is connected to the junction bus 19 connected to the chip output terminal 31 for every wiring, and a data electrical potential difference is changed into the logical level suitable for the logical circuit by TFT. The output of the level-shifter circuit 120 is inputted into the input terminal 109 of a shift register 122, respectively. It connects with a part for the number of stages equivalent to the block count which divides the data for one line, and a serial, and the shift register 122 constitutes the shift register train.

[0086] A shift register 122 operates with the shift clock 162 from the transfer control circuit 26. The shift clock 162 synchronizes with the memory chip block change signal 131 of a memory chip 12.

[0087] Drawing 24 is the explanatory view showing actuation of a signal input selection circuitry. The shift register train of the signal input selection circuitry 121 incorporates the data of each block inputted into the input terminal whenever the shift clock changed, and shifts them to the right one by one. If a shift action is repeatedly completed to block 1-h, the data of the k-th line will be sampled. If the Rhine latch control signal 132 is impressed at this time, the data for one line will be transmitted to the Rhine latch 23. Then, a display action is performed by the liquid crystal gradation drive circuit 24 like an example 1.

[0088] To having been required for the level shift circuit of an example 1 by one line, the level shift circuit of an example 2 can be managed with 1 block, and can reduce power consumption. The signal wiring of a 640x480-pixel panel will become 640 circuits if a level-shifter circuit is arranged after those with 640, and a selection latch circuit, but when it arranges after a signal input selection circuitry, only the number of the junction buses 19 is required, for example, if the number of junction buses is 40, it is good in 40 circuits and, specifically, the power consumption of this part can be cut down to 1/80.

[0089] Moreover, since the wiring intersection of a signal input selection circuitry can be decreased, increase of the power consumption by a logic electrical potential difference becoming high can be offset.

[0090] [Example 3] Drawing 25 shows the cross-section structure of the liquid crystal panel by other examples. The liquid crystal panel of a reflective mold is shown to the liquid crystal panel of the

transparency mold of drawing 4 . In this example, the reflective display electrode 141 is used as a display electrode, using a dichroic polymer dispersed liquid crystal or guest host mold liquid crystal as high reflective liquid crystal 140 used for a display.

[0091] The outline structure of a picture element part is shown in drawing 26 . The picture element part of a display 29 is an intersection of the shape of a matrix of the gate wiring 110 and the drain wiring 106, and consists of pixels TFT142 linked to these. The reflective mold display electrode 141 is formed with the metal thin film with a high reflection factor, and when the liquid crystal driver voltage impressed to the drain wiring 106 is inputted into a selection pulse by the gate wiring 110, it drives liquid crystal 140 by flowing through a drain electrode and the display electrode 141.

[0092] By using high reflective liquid crystal, a back light becomes unnecessary, and power consumption serves as only the image memory chip 12 and the TFT circumference circuit 40, and can perform much more reduction of power consumption.

[0093] [Example 4] Next, the example of the computing system which applied the liquid crystal display of this invention is explained. The example of the computing system by this invention is shown in drawing 27 . A keyboard 154 and a liquid crystal display 3 for this system to input CPU150 which carries out data processing of the information, the memory device 151 which memorizes data, I/O153 which controls data I/O with the system exterior, the controller 152 which performs control of a system, a command, etc. are mutually connected through the system bus 158. It is the configuration that an image memory chip is mounted in a liquid crystal panel, and it is only supplying the modification part and the indicative data from CPU150 can update the image display of a display as the liquid crystal display 3 was explained to the example 1 thru/or the example 3.

[0094] The liquid crystal display 3 of this system is connected to the independent display power source 157. System power 155 is a power source which drives except display 3, and has an electric power supply to each part controlled by CPU150 and the power control section 156 corresponding to the situation of a key input or a system bus 158. Usually, all components are worked and an input, an information operation, a display, etc. are performed. When restricted to a part of actuation, by CPU150, under count etc. can control system power, can intercept energization of an element [**** / un-], and can reduce power consumption.

[0095] Furthermore, when waiting for an input is carried out exceeding fixed time amount, system power 155 can be intercepted, CPU150 can be stopped, only a liquid crystal display 3 can be worked, and the screen display till then can be maintained. It can key from the condition and a system can also be rebooted.

[0096] Since the conventional liquid crystal display module always needs to supply an indicative data from CPU or a controller, if CPU or the controller of a computing system is stopped, the contents of a display will also disappear. However, since the image memory for the indicating equipment itself to hold an indicative data is built in according to the computer system of this example, when there is no need for operation of other equipments of a system, even if it intercepts the electric power supply, a display action can be maintained, and it is effective in the ability to reduce the power consumption of a system sharply.

[0097]

[Effect of the Invention] Since according to this invention the image memory chip in which an image memory and its read-out control circuit were formed is mounted on the same substrate as a liquid crystal module, wiring of many connections is formed on a substrate and the parallel transmission of the indicative data from an image memory to a liquid crystal module is carried out, it is effective in the ability to reduce a transfer frequency sharply compared with the conventional serial transmission, and reduce power consumption.

[0098] Moreover, by reduction of a transfer frequency, even if the mobility of the circumference circuit constituted on a TFT substrate is low, required circuit actuation is secured, and there is effectiveness which can improve the definition of an image.

[0099] Furthermore, since an indicative data is held to an image memory and a display action is made possible also when there is no writing from drawing control circuits, such as CPU, rewriting of an

indicative data is good only in the modification part of the contents of a display. For this reason, CPU can process other business to a period without a display and modification of a static image, or can also interrupt current supply other than a display to it, and can improve the processability and power saving equipped with a liquid crystal display in a minicomputer etc. at it.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] This invention relates to a liquid crystal display, and relates to the liquid crystal display which mounted the image memory chip on the TFT substrate of a liquid crystal display panel.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] The method which forms a matrix circumference circuit on a glass substrate, using a thin film transistor as a drive circuit of a small and high definition liquid crystal display panel is learned. For example, it is reported to 348-345 pages of "EKUSU ten dead abstract OBU 1997 International conference-on solid-state device and MATERIARUSU." Moreover, detail of a active-matrix drive method and a liquid crystal display module is given to "the liquid crystal display technique (Sangyo Tosho Publishing)" of the work edited by Shoichi Matsumoto in detail.
[0003] The configuration of the conventional TFT-liquid-crystal display module is shown in drawing 2 . In information machines and equipment, such as a personal computer, the indicative data which CPU30 or a display-control circuit becomes from the coordinate of each dot of a dot-matrix display and the combination of gradation data about a display day is generated. The image memory 13 which stores an indicative data is another arranged in the liquid crystal display 3 which really formed the display 29 and the circumference circuit section of a TFT active matrix with CPU and the display-control circuit.
[0004] In order to reduce a wiring number, serial transmission of the data from the image memory 13 to the liquid crystal display module 3 is carried out. A display-control circuit is read from an image memory 13 per several dots, and after it carries out rearrangement processing to a serial, it is sent to a liquid crystal display module as serial transmission data 8. Serial data is the serial parallel conversion circuit 9, it is again rearranged into the parallel signal of the data for one line, is changed into the signal wiring driving signal of a active matrix by the Rhine latch and the liquid crystal gradation drive circuit 10, and drives a display 29.
[0005] Between the image memory of this system, and a display-control circuit, and between a display-control circuit and a liquid crystal display module, the data for all pixels are usually transmitted at high speed by the repeat in a cycle of 60-75Hz.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] Since according to this invention the image memory chip in which an image memory and its read-out control circuit were formed is mounted on the same substrate as a liquid crystal module, wiring of many connections is formed on a substrate and the parallel transmission of the indicative data from an image memory to a liquid crystal module is carried out, it is effective in the ability to reduce a transfer frequency sharply compared with the conventional serial transmission, and reduce power consumption.
[0098] Moreover, by reduction of a transfer frequency, even if the mobility of the circumference circuit constituted on a TFT substrate is low, required circuit actuation is secured, and there is effectiveness which can improve the definition of an image.
[0099] Furthermore, since an indicative data is held to an image memory and a display action is made possible also when there is no writing from drawing control circuits, such as CPU, rewriting of an indicative data is good only in the modification part of the contents of a display. For this reason, CPU can process other business to a period without a display and modification of a static image, or can also interrupt current supply other than a display to it, and can improve the processability and power saving equipped with a liquid crystal display in a minicomputer etc. at it.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] With the above-mentioned conventional technique, the indicative data of all pixels must be transmitted for every frame time to a liquid crystal display module. It increases, so that the number of pixels of the transfer rate at this time increases, for example, with a 1024x768-pixel configuration, a transfer with a high speed of about 50MHz is needed. For this fast transfer, LSI in a module must operate at this rate. Since a CMOS circuit is used, as for the basic circuit built in LSI, power consumption increases with a working speed. For this reason, definition followed the liquid crystal module of this method on becoming large, and it had the problem said that power consumption increases.
[0007] Moreover, the TFT circumference circuit technique which constitutes the circumference circuit of the liquid crystal display section is used with the small display. However, compared with the circuit of LSI formed on Si chip, since the polycrystal thin film Si and the vacuum evaporationo film SiO2 are used as gate dielectric film, mobility is low and a circuit working speed is also slow. For this reason, highly-minute-izing by the conventional TFT circumference circuit was difficult.
[0008] The purpose of this invention is to offer the liquid crystal display which the data transfer frequency from an image memory to a liquid crystal module can fall sharply, and can reduce clock frequency and power consumption in view of the trouble of the conventional technique, and can be miniaturized.
[0009] Moreover, the liquid crystal display which mounted the image memory is connected, and it is in offering the computing system which can improve reduction of power consumption, and the processability of CPU.
[0010] Furthermore, the indicative data for level 1 Rhine is memorized at least, and it is in offering the possible image memory of division read-out corresponding to the number of output signal lines.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] This invention for attaining the above-mentioned purpose The substrate of a pair at least with transparent one side, It has the liquid crystal layer arranged between this substrate. Two or more scan [one side / of said substrate] wiring, In the liquid crystal display which has the display electrode connected to two or more signal wiring, two or more thin film semiconductor components formed corresponding to the intersection of those wiring, and two or more of these semiconductor devices, and ********** in another side of said substrate On one [said] substrate, the connection which has a junction bus for transmitting an indicative data in said signal wiring is formed, and it is characterized by coming to mount the image memory chip which memorizes the indicative data for the horizontal of one line at least through said connection.
[0012] Moreover, the signal side circumference circuit for driving said liquid crystal and a scan side circumference circuit are formed on the TFT substrate which constitutes said liquid crystal panel, and it is characterized by coming to connect the input and said junction bus of said signal side circumference circuit.
[0013] Moreover, while said image memory chip carries out address attachment of said indicative data and memorizes it to a reading horizontal direction one by one The store circuit as for which the indicative data for the horizontal of one line of the same address is read and made to coincidence, The memory output latch holding the indicative data for one line, and the latch selection circuitry which chooses said output latch's output and is connected to said junction bus, While controlling to read the indicative data from said store circuit, and to latch to said memory output latch for every level Rhine one by one, it is characterized by coming to constitute the read-out control circuit which controls selection connection of said latch selection circuitry on semi-conductors, such as a silicon chip.
[0014] Since according to the description of this image memory chip it outputs to the signal junction bus with the signal line of the number of fixeds number of line of arbitration alternatively and the indicative data for one line can be transmitted to it, it is effective also as general-purpose image memory.
[0015] Moreover, a signal selection means to incorporate the indicative data for ****** level 1 Rhine for the input circuit which makes selection connection with said junction bus in said signal side circumference circuit one by one (for example, block electronic switch), The level shifter which transforms into the logic electrical potential difference of said signal side circumference circuit the logic electrical potential difference of said indicative data expressed by binary data, It has the liquid crystal driver voltage generating circuit which changes an indicative data into the liquid crystal driver voltage of an analog with the Rhine latch holding the indicative data for the horizontal of one line. It comes to prepare for said memory chip or said liquid crystal panel the transfer control circuit controlled to synchronize selection actuation of the both sides of said latch selection circuitry of the said signal selection means and said image memory of said signal side circumference circuit.
[0016] Moreover, selection actuation of said signal selection means of said latch selection circuitry of said image memory and said signal side circumference circuit is characterized by performing connection and a change of a block unit, when dividing and transmitting the indicative data for the horizontal of one line to two or more blocks.

[0017] Or said signal selection means of said signal side circumference circuit **** signal wiring for said horizontal of one line to two or more signal wiring blocks which consist of the same number as said junction bus, and is characterized by constituting so that selection connection of this block and said junction bus may be made using a semi-conductor analog switch.
[0018] Moreover, said level shifter is characterized by connecting between said junction bus and said signal selection means or after said signal selection means.
[0019] According to this invention, the image memory was mounted on the liquid crystal panel in which the display and TFT circumference circuit of a TFT active matrix were formed, and parallel connection of an image memory and a circumference circuit is realized on a substrate. For this reason, since an indicative data is always held at an indicating-equipment side, rewriting of an indicative data requires only a modification part, and the transfer frequency from CPU to an indicating equipment can reduce it sharply. Moreover, since it becomes the parallel transfer of the horizontal of one line at the maximum, a transfer frequency falls, and the data transfer from an image memory to a circumference circuit can reduce the clock frequency and power consumption of the whole display sharply.
[0020] In the computer system to which this invention which attains the purpose besides the above connected CPU, memory, I/O I/O, and an indicating equipment by the system bus, said indicating equipment is mounted in the liquid crystal display panel and this panel of an active matrix, and from said CPU, the indicative data of a modification part is written in and it is characterized by new or having the image memory which memorizes a part for the horizontal of one line at least.
[0021] Moreover, it is characterized by preparing ** / power control section which carries out ** for supply of drive power according to the operating status of the system power which supplies drive power, and components other than said display in each of the component in a system.
[0022] The basic configuration of the liquid crystal display by this invention is shown in drawing 1 . The indicative data and control signal from CPU30 are transmitted to a display 3 through the data address bus 1 and the control signal line 2. The indicating equipment 3 mounts the image memory chip 12 in the connection 5 which formed the TFT circumference circuit 40 which used the display 29 of a TFT active matrix, and Polycrystal TFT on the TFT substrate, and was formed on the TFT substrate.
[0023] The indicative data transmitted from CPU30 is written in the image memory 13 built in the image memory chip 12. A change of the contents of a display is made by rewriting the data of the part corresponding to a modification pixel from CPU30.
[0024] The read-out control circuit 18 reads the indicative data of an image memory 13 collectively for every one line of a matrix, transmits it to the Rhine memory parallel interface 4, processes rearrangement suitably and transmits it to the TFT circumference circuit 40 with a control signal through the connection 19 including the junction bus for two or more pixels. Processing of rearrangement is needed, when 1 time of the number of parallel transfers divides one line into multiple times and performs it.
[0025] The transfer control circuit 26 controls actuation of the TFT circumference circuit section 40. First, the indicative data sent from the image memory chip 12 side is rearranged with the parallel input interface 6, and is changed into the signal wiring driver voltage of a active matrix by the liquid crystal gradation drive circuit 7. This parallel input interface 6 and the liquid crystal gradation drive circuit 7 are equivalent to the signal side circumference circuit 32. Synchronizing with the scan signal from the scan side circumference circuit 33, signal wiring driver voltage is impressed to a display 29, and the liquid crystal of a picture element part is driven.
[0026] Thus, an image memory chip is carried on the substrate which forms a liquid crystal display panel, connection of the number of multipoints of high density is made between a chip and a substrate, and parallel transmission of the data of all pixels is periodically carried out between an image memory and a TFT circumference circuit. Therefore, the clock frequency of a display can decrease sharply and low-power-ization can be attained.
[0027] Moreover, since CPU should transmit only the pixel data which change the contents of a display to a display, write-in processing of CPU can decrease sharply and expansion of the processability of CPU and reduction of power consumption are attained. This description has a large merit at small

machines, such as a notebook computer.
[0028] Moreover, by reduction of the clock frequency of the drive circuit of a display, a high definition display is attained also by the circumference circuit on a TFT substrate with actuation slower than Si chip, modular mounting components mark are reduced, and it can miniaturize.
[0029]
[Embodiment of the Invention] Hereafter, two or more examples of the liquid crystal display of this invention are explained to a detail, referring to a drawing. In addition, the same sign is given to the equivalent element through each drawing.
[0030] [Example 1] The liquid crystal display structure of a system of an example 1 is shown in drawing 3 . The liquid crystal display of this example consists of image memory chips 12 mounted in the connection 5 formed on the same TFT substrate as the liquid crystal display panel 11 which consists of a display 29 with the pixel of the active matrix formed on the TFT substrate, and its TFT circumference circuit.
[0031] The liquid crystal display panel 11 is based on the configuration on the conventional TFT substrate. A transistor component is formed in the intersection of the two or more scan wiring and signal wiring which intersect perpendicularly mutually. The display 29 which **** liquid crystal with the display electrode and counterelectrode which were connected to the gate electrode and drain electrode of this component, forms a pixel, and comes to arrange this pixel to the above-mentioned intersection in the shape of a matrix, Since the pixel of an active matrix is driven, it consists of a scan side circumference circuit 33 which supplies the signal side circumference circuit 32 and scan signal which supply a status signal. The signal side circumference circuit 32 is different from the conventional configuration so that it may mention later.
[0032] The junction bus 19 of a connection 5 etc. is formed on a TFT substrate of a CMOSTFT formation process, connects the outgoing end of the image memory chip 12, and the input edge of the signal side circumference circuit 32, and makes the parallel transmission of a status signal possible.
[0033] While the image memory chip 12 is formed on Si chip, reading the indicative data for one frame one by one in a part for the horizontal of one line, and this example at least, carrying out address attachment horizontally and memorizing The image memory 13 memorized possible [coincidence read-out of the indicative data for one line of the same address], The indicative data of an image memory 13 is read one by one with the memory output latch 16 holding the indicative data for one line. The read-out control circuit 18 controlled to latch the read indicative data to the memory output latch 16 for every level Rhine one by one and the latch selection circuitry 17 which makes selection connection of latch's 16 output into the junction bus 19 are provided.
[0034] Moreover, the transfer control circuit 26 controlled by the both sides of the latch selection circuitry 17 and the signal side circumference circuit 32 of the liquid crystal display panel 11 to synchronize selection actuation is formed. In addition, the transfer control circuit 26 is not the image memory chip 12, and may be established in the liquid crystal display panel 11 side.
[0035] The cross-section structure of the outline of a liquid crystal display is shown in drawing 4 . The liquid crystal display panel 11 seals liquid crystal 43 with the liquid crystal seal 44 among these, puts it with two polarizing plates 45 from those outsides, and comes to combine a back light 46 with the TFT substrate 41 which forms TFT, and the opposite substrate (glass substrate) 42 in which the transparence electric conduction film 49 containing a color filter 48 and tin oxide was formed on the front face. The transistor component from which the display 29 only illustrating a part serves as a drive circuit at the substrate 41 of the liquid crystal 43 bottom is formed in the shape of a matrix. The circumference circuit 40 of a display 29 is formed in the substrate 41 of the outside of the field which is pinching liquid crystal 43.
[0036] Furthermore, on the TFT substrate 41 of the outside between polarizing plates 45, the image memory chip 12 is mounted and the junction bus 19 which connects the circumference circuit 40 with a chip 12 is formed. It connects with the chip input terminal 37 through wiring on the TFT substrate 41 etc., and the image memory chip 12 is connected with the bus wiring 38 using a flexible printed circuit board etc.

[0037] Alkali free glass is used for a TFT substrate as Si film, and the low-temperature polish recon by the laser annealing grown method is used for formation of a TFT substrate as the Si crystal film formation approach. Or polycrystal Si film, such as elevated-temperature polish recon by the solid phase grown method, is used using a quartz-glass substrate. The doping method is combined with this and TFT of pchnch is formed on the same substrate at coincidence.
[0038] The conventional LSI process can constitute the image memory chip 12 with a connection part with the TFT substrate 41. Moreover, connection by ** pitch wiring of 100 micrometers or less is possible for the connection with the bus wiring 38, and the image memory chip 12 and the TFT substrate 41 by using ANISORUMU which is the goods of the anisotropy electric conduction film of Hitachi Chemical Co., Ltd.
[0039] Next, the configuration and actuation of the liquid crystal display of this example are explained to a detail according to drawing 3 . Through the address bus wiring 34 and the data bus wiring 35, the indicative data changed into the pixel address and the gradation data for every pixel is inputted into the memory chip 12 of an indicating equipment 3 by CPU30 with the control signal for the data transfer timing control by the control signal line 36, and is written in an image memory 13 through the data-line decoder 14, the word line decoder 15, and the data interface circuit 50.
[0040] In addition, conversion to the gradation data for every dot is good also by logical devices which assign the memory area according to individual every [1 dot of a display, or] two or more dots, such as a display controller which has the function to generate an indicative data and the address in a bit map addressing format.
[0041] The indicative data memorized in the image memory 13 controls word line DEKOTA 15 from the read-out control circuit 18, only several display data bit minutes for the horizontal of one line of an image memory 13, carries out a sequential sampling and reads it to the memory output latch 16. The indicative data for one line latched to the memory output latch 16 is divided into two or more blocks, is chosen at a time in predetermined sequence by 1 block of latch selection circuitries 17, and is outputted from the chip output connection terminal 31 with the number for 1 block.
[0042] The indicative data outputted in the block unit is inputted into the signal side circumference circuit 32 of the liquid crystal display panel 11 on the same substrate through the junction bus 19 formed on the TFT substrate from a memory chip 12. Actuation of the signal side circumference circuit 32 is controlled by the transfer control circuit 26.
[0043] First, the block electronic switch 20 outputs the data of a block unit for every block chosen from the selection latch circuit 21. The logic signal level of an indicative data is changed into the logic electrical potential difference of a TFT circumference circuit by the level shifter 22 at this time. When the indicative data for one line is held by transmitting every block one by one at the selection latch circuit 21, it is transmitted to the Rhine latch 23 all at once.
[0044] The liquid crystal driver voltage generating circuit 24 changes an indicative data into a liquid crystal gradation electrical potential difference, and drives the drain wiring 106 of a display 29. On the other hand, the gate wiring 110 of a display 29 is driven by the gate wiring drive circuit 27 and the scan side circumference circuit 33 which consists of a scan shift register 28. The shift clock 113 and the frame start signal 114 used as scan timing are supplied from the transfer control circuit 26. The above transfer operation of one line is carried out by all Rhine to an one-frame within a time, and the display of one screen is realized.
[0045] In the above-mentioned configuration, the number of data of 1 block increases, so that there are many bus numbers of the junction bus 19, and the count of a data transfer can be decreased. Although it depends for a bus number on the precision of processing equipment, since it becomes connectable [50 micrometer pitch] with the chip of 5mm angle in the present equipment, the ejection of 300 terminal extent becomes possible by using 100 terminals and three sides per side. Since terminal formation of about further 3 times is possible by using a terminal configuration as an alternate pattern, the connection whose 1 block is about 300 bits is easy.
[0046] The example of application of the liquid crystal panel of practical use is explained. By the 640x480-pixel panel, to transmit 640 pixels for one line, and a gradation signal with a color [RGB

each] of 6 bits, it is necessary to transmit 640x3x6=11520 bit. Therefore, the count of a transfer in the case of a 300-bit parallel transfer becomes 38.4 times. Since the period of one line is set to 1/70/480=29.8microsecond by the transfer time in the case of 70Hz frame frequency, the transfer frequency in this case is set to 1.3MHz. Since the dot clock of the conventional example is set to 20MHz or more, it turns out that it becomes sharp frequency reduction. Moreover, much more reduction is possible by dividing an image memory chip into plurality, synchronizing it with it, and driving.

[0047] The detailed configuration and actuation of each circuit are explained. The configuration of an image memory chip is shown in drawing 5 . The image memory chip 12 is connected with a system bus through the address bus wiring 34, the data bus wiring 35, the bus wiring 38 into which the control signal line 36 was packed, and the chip input connection terminal 37.

[0048] The word line 62 to arrange a memory cell 63 in the shape of a matrix, and for an image memory 13 choose each memory cell is connected to word line DEKOTA 15 common to a line writing direction. The bit line 65 which writes in data is connected to the bit line drive circuit 51 common to the direction of a train. The bit line drive circuit 51 is written in and consists of the data interface 50 and data-line DEKOTA for control. It connects with a sense amplifier 64, the cel for one line which corresponds if a word line is chosen is chosen, and each of a bit line 65 outputs the condition of a cel to a sense amplifier 64 all at once.

[0049] The condition of a bit line 65 is changed into data by the sense amplifier 64, and it is read to the memory output latch 16 by the memory latch control signal 131, and connects with the latch selection circuitry 17. It connects with two or more chip output terminals 31, and the output of the latch selection circuitry 17 is connected with a liquid crystal panel 11 through the junction bus 19.

[0050] Among these, the bit line drive circuit 51 for writing in a memory cell 63 and word line DEKOTA 15 are the same as that of the method of a dual port memory chip, and good.

[0051] The control signal for controlling the write-in actuation to memory 13 is generated by the read-out control circuit 18, and is supplied to word line DEKOTA 15 and the bit line drive circuit 51. Moreover, the memory latch control signal 131, the memory chip block change signal 130, and the control signal of the transfer control circuit 26 which controls actuation of a TFT circumference circuit are also generated. The transfer control circuit 26 outputs the block selection signal 84, the block latch signal 88, the Rhine latch signal 132, the shift clock 113, and the frame start signal 114. In addition, the control signal to a TFT circumference circuit has added and transmitted the number required for the junction bus 19.

[0052] The circuitry of a memory cell is shown in drawing 6 . The memory cell 63 was constituted by six transistors and has connected the VDD terminal 66 and the VSS terminal 67 to a power source. The bit terminal 69 and the reversal bit terminal 70 which output and input a reversal signal mutually [in order to output and input the WORD terminal 68 for choosing a cel and data] are connected to the word line 62 of a matrix, and a bit line 65, respectively.

[0053] The circuitry of a sense amplifier is shown in drawing 7 . If a sense amplifier 64 is constituted by five transistors and a power source VDD and bias voltage VCS are impressed, it will impress the bit signal and reversal bit signal which are reversed mutually to an input terminal 71, and will obtain the data output 72 which has the amplitude of supply voltage.

[0054] Memory output latch's circuitry is shown in drawing 8 . The input edge is connected to the data output terminal 72 of a sense amplifier 64, and two or more latch circuits 97 arranged at juxtaposition are latched all at once with the memory latch control signal 131.

[0055] The configuration of a latch circuit is shown in drawing 9 . A latch circuit 97 consists of two inverters 90 with a CMOS transistor, and the two transfer gates 91 and the control inverters 92. Only when the memory latch control signal 131 inputted into the control terminal 94 from the read-out control circuit 18 is logic "forward", the transfer gate 91 serves as open, and the data from the sense amplifier 64 inputted into the input terminal 93 drive an inverter 92, and change the condition of the latch output 95. When the memory latch control signal 131 is logic "negative", an output state does not change but holds data.

[0056] The configuration of a latch selection circuitry is shown in drawing 10 . The latch selection

circuitry 17 makes sequential connection of the data line 134 for one line of the total N bit from the memory output latch 16 into m output buses 82 through the analog switch 135 which used the transfer gate. For this reason, the data line is divided every m, it considers as the output block 81 of block 1 - h, and selection connection is multiplexed and made for every output block. Since the data line of N book is divided into h blocks corresponding to m output buses, it becomes the relation of block count h=N/m.
[0057] The block 81 which connects with the output bus 82 and is outputted is performed by control of an analog switch 135. For this reason, only a specific output block is alternatively connected by packing a selection-signal input terminal by using an analog switch 135 as the block analog switch 83 for every block, impressing a logic "forward" signal only to any that one, and impressing a logic "negative" signal to others. The memory chip block change signal 130 is supplied from the read-out control circuit 18, and since the control signal which the polarity reversed for control of an analog switch is the need, an inverter 85 is connected every change signal 130. The output bus 82 is connected to the junction bus 19 through the chip output connection terminal 31.
[0058] Next, the configuration and actuation of the signal side circumference circuit 32 and the scan side circumference circuit 33 are especially explained to a detail about the liquid crystal panel of this example.
[0059] The block electronic switch 20 of the signal side circumference circuit 32 transmits the indicative data inputted through the junction bus 19 from the image memory chip 12 in order of a block, and the selection latch circuit 21 carries out the rearrangement of the indicative data for one line.
[0060] The configuration of a block electronic switch is shown in drawing 11 . The output wiring 136 for one line (N book) of the block electronic switch 20 is divided into 1-h blocks, and is connected to the junction bus 19 through the TFT analog switch 161 and the input bus 86 for 1 block (m) which are constituted by CMOSTFT.
[0061] An analog switch is packed every m pieces and constitutes the TFT block analog switch 160. The control signal of a switch 160 generates the control signal of amphipathy required for analog switch control with an inverter 89 in common for every block. By impressing a logic "forward" signal only to any one, and impressing a logic "negative" signal to others with the block selection signal 84 supplied from the transfer control circuit 26, each block is chosen in predetermined order and closing motion of a switch is connected with the input bus 86. The indicative data expressed by the output wiring 136 of the block output 87 connected with the input bus 86 fits the logical level of the output signal of an image memory 13 to the logical level of a thin film transistor circuit by the level shifter 22, and is sent to the selection latch circuit 21.
[0062] The circuitry of a selection latch and the Rhine latch is shown in drawing 12 . This drawing (a) is the selection latch circuit 21, it arranges two or more latch circuits 97, packs a latch control signal for every block which consists of m, and is constituted possible [the latch of a block unit]. With the block latch signal 88 from the transfer control circuit 26, the data of the same block are latched synchronizing with the block electronic switch 20. The output of the selection latch circuit 21 is connected to the Rhine latch circuit 23. This drawing (b) is a latch circuit 97, and is constituted by CMOSTFT. However, since it becomes the same configuration as the latch circuit of drawing 9 , the sign of a circuit element supposes for convenience that it is the same.
[0063] Drawing 12 (c) is the Rhine latch 23, and is carrying out parallel connection of the same latch circuit 97 as drawing 12 (b) by N bit. Package connection is made and the latch control signal edges 94 of all the circuits 97 sample the indicative data for one line all at once with the Rhine latch signal 132 from the transfer control circuit 26.
[0064] The circuitry of a level shifter is shown in drawing 13 . A level shifter 22 consists of six transistors. The input signal from the block electronic switch 20 is inputted into the reversal signal and four transistor circuits in all by the inverter 90, and the logic electrical potential difference is amplified to the electrical potential difference of a power supply terminal 99.
[0065] Thus, a level shifter 22 is connected behind the block electronic switch 20, and the logical level of the output signal of an image memory 13 is fitted to the logical level of a TFT circuit. Consequently, power consumption can be reduced for the following reasons.

[0066] As for the block electronic switch 20, the output wiring 136 of m junction buses 19 and N book constitutes ** / matrix by which ** is carried out from an analog switch, and crossover capacity is formed in this wiring intersection. In order to change a signal to a high speed by the matrix, it is necessary to see from the image memory chip 12 and to carry out the charge and discharge of the crossover capacity to a high speed. The power consumption at this time is proportional to capacity value, and proportional to the square of signal amplitude. Then, power consumption can be reduced by lowering the driver voltage of the block electronic switch 20.
[0067] In this example, the image memory chip 12 is what was formed by LSI on a silicon substrate as a semiconductor device, and is used less than [logic electrical-potential-difference 5V] for high integration. On the other hand, operating voltage of the TFT circuit of a liquid crystal panel 11 must be made higher than liquid crystal driver voltage, and about 8-16V is specifically needed. Then, up to the block electronic switch 20, a logic electrical potential difference drives on the logic electrical potential difference of 3.3-5v, and an image memory, carries out the pressure up of the logic electrical potential difference to 10-12V by the subsequent level shifter 22, and enables the liquid crystal drive. Consequently, reduction and high-speed operation of power consumption are made possible.
[0068] In this example, since the switch change method is used for the block electronic switch 20, regardless of the logic electrical potential difference of an indicative data, the change of a signal is possible. In addition, the change of a signal is possible also by the combination of two or more logical circuits. In that case, it is necessary to carry out a level shift to the logic electrical potential difference for high-speed logical circuits constituted from the input section of the block electronic switch 20 by TFT.
[0069] The configuration of a liquid crystal driver voltage generating circuit is shown in drawing 14 . a input terminals 100 into which an a-bit digital gradation signal is inputted with a binary number are connected to the gradation voltage selection switch 104 using the transfer gate 103 through the DEKOTA circuit 101 which combined the logical circuit, and the liquid crystal driver voltage generating circuit 24 is connected with the drain wire the output line 106 of whose is the signal wiring of a display 29. The gradation voltage selection switch 104 is connected to the gradation electrical-potential-difference bus 105 which consists of wiring of a Norimoto of 2, and each wiring of a bus 105 is connected to the gradation power source 47 of different amplitude corresponding to gradation.
[0070] Therefore, the a-bit digital gradation signal connected to the input terminal 100 expresses the gradation data corresponding to the gradation number of a binary number notation. one gradation control signal corresponding to the gradation number of a binary number notation by the DEKOTA circuit 101 -- a Norimoto of 2 -- it chooses from a number of gradation control signal 102. By making it flow only through the one transfer gate 103 of the gradation voltage selection switch 104, a gradation control signal connects 1 and the output line 106 of the gradation electrical-potential-difference bus 105 to which the specific gradation power source was connected, and outputs a gradation electrical potential difference. Thereby, corresponding to the a-bit indicative data showing 1-pixel gradation, it is changed into the liquid crystal driver voltage to which the permeability of liquid crystal is changed, and is outputted to the drain wire of a picture element part from an output line 106.
[0071] Next, the scan side circumference circuit 33 of drawing 15 explains the configuration of a shift register 28 and the gate wiring drive circuit 27. A shift register 28 connects the multistage shift register circuit 112 to a serial, and the shift clock 113 of the frame start signal 114 and amphipathy is supplied to an input from the transfer control circuit 26. The gate drive circuit 27 is constituted by the inverter train 111 which carried out the series connection of the inverter one by one with big gate width, inputs the output of each stage of a shift register 28, and drives gate wiring of a display 29 at a high speed.
[0072] The circuit diagram of a shift register is shown in drawing 16 . A shift register 28 connects to a serial many shift registers 112 which consist of eight inverters 107 and the eight transfer gates 108, and is constituted. By driving with the shift clock 113 with which polarities differ mutually [two phases], it is delayed for every sequential shift clock, and an input signal 109 is outputted to the gate wiring 110.
[0073] Besides above, the read-out control circuit 18 and the transfer control circuit 26 which generate various kinds of above-mentioned control signals are constituted by the combination of the logical

circuit which used CMOS, respectively. It is the conventional technique fundamentally and detailed explanation is omitted.

[0074] Next, actuation of the liquid crystal display of this example is explained. Drawing 17 is a timing diagram which shows the write-in actuation to an image memory from CPU. As mentioned above, the address and data are specified from CPU30, and the memory select signal and the read-out control signal are included in the control signal.

[0075] If a memory select signal becomes logic "0", an image memory will be chosen and the writing to an image memory 13 will be attained. Then, the condition of a data bus in case a write-in control signal changes from logic "0" to logic "1" is written in the memory cell 63 of the appointed address of an image memory. Thus, the writing of the indicative data to an image memory 13 is performed by the same procedure as other memory connected to CPU, and does not have the conventional personal computer carrying a liquid crystal display, etc. and the changing place.

[0076] Next, read-out of an indicative data is explained. Drawing 18 is a timing diagram which shows the read-out actuation of one frame to the memory output latch from an image memory. If word line DEKOTA 15 operates with directions of the read-out control circuit 18 and it chooses 1 of a word line 62 - one n at a time one by one, a part for the data of one line of the memory cell 63 connected to the word line 62 will be inputted into a sense amplifier 64 through a bit line 65, and will be changed into digital data. If this is inputted into the memory output latch 16 one by one and is latched with the memory latch control signal 131, the output latch's 16 output will change. The above read-out actuation is repeated to 1 frame time from the 1st line to the n-th line of the scanning-line number of one screen, and a series of actuation is further repeated for every frame time.

[0077] Drawing 19 is the explanatory view showing actuation of a latch selection circuitry. The latch selection circuitry 17 outputs the memory output latch's 16 output for one line to m chip output terminals 31. A part for an indicative-data hxm bit for the horizontal of one line of scanning-line k Motome is held like the array of the illustration to the memory output latch 16. This is divided into m bits and h blocks, and it chooses in order from the 1st block to h blocks with the memory chip block change signal 130 supplied from the read-out control circuit 18. Thereby, it can connect with the output bus 82 one by one to block 1-h, and the indicative data for one line is outputted to the chip output terminal 31 and a pan per block to the junction bus 19.

[0078] Drawing 20 is the explanatory view showing actuation of the selection latch circuit which incorporates an indicative data through a block electronic switch. The data from the sequential block 1 to Block h are outputted to the junction bus 19. If the block selection signal 84 is supplied to the block electronic switch 20 from the transfer control circuit 26, the block latch signal 88 is supplied to the selection latch circuit 21 and the selection signal and block latch signal of an applicable block are made into logic "forward" synchronizing with this, data will be incorporated by the selection latch circuit 21 to which the selection block was connected, and the output will be rewritten. In this case, it is changed into the level of an about [10-12v] TFT logical circuit by the level shifter 22 connected to the input side of each selection latch circuit 21.

[0079] Thus, after renewal of sequential of the data arrangement on a selection latch is partially carried out like illustration and rewriting to 1-h blocks finishes, the data of the k-th line are arranged on a selection latch. In addition, since read-out actuation of the image memory chip 12 and actuation of the block electronic switch 20 and the selection latch circuit 21 are performed synchronously, the indicative data of one line on the memory output latch 16 of an image memory 13 is transmitted to the selection latch circuit 21 within 1 horizontal-scanning period.

[0080] Drawing 21 is a timing diagram which shows actuation of the Rhine latch. The data of scanning-line 1 duty are updated and supplied to the Rhine latch's 23 input for every 1 level period from the selection latch 21. This input data is incorporated with the Rhine latch control signal 132 from the transfer control circuit 26, and the Rhine latch output data are updated. It connects with the liquid crystal driver voltage generating circuit 24, and the Rhine latch output is changed into liquid crystal driver voltage in an instant, and is supplied to drain wiring of a correspondence pixel from an output line 106.

[0081] Actuation of a display 29 is the same as usual. The scan pulse to which each picture element part

by which the matrix configuration of the display 29 is carried out carried out the sequential shift of the pixel of 1 level Rhine from the gate wiring 110 is impressed from a scan side circuit. Moreover, in a signal side circuit, synchronizing with a scan pulse, the liquid crystal driver voltage for one line is impressed from drain wiring of each pixel from the liquid crystal driver voltage generating circuit 24, and the pixel display of the horizontal of one line is performed.

[0082] As mentioned above, according to the liquid crystal display of this example, the image memory chip mounted on the display panel memorizes the indicative data from drawing control circuits, such as CPU, by the bitmapped image, reads the digital indicative data for one line to coincidence, takes a synchronization by the transfer control circuit, and carries out a sequential output into a junction bus for every two or more pixels of a block unit. This indicative data is supplied to the circumference drive circuit which used the thin film TFT and was formed with the display on the display panel through a junction bus. A circumference drive circuit takes a synchronization by the transfer control circuit, incorporates an indicative data one by one to the selection latch for one line, transmits it to the Rhine latch, and holds the data for one line. It changes into the gradation electrical potential difference which impresses the digital gradation data of each dot to the liquid crystal of a pixel using this data.

[0083] Consequently, the interface of an image memory and a display can be simplified, and since the transfer clock for transmitting the data which are one line can be reduced, the power consumption of a display can be reduced sharply. Moreover, a liquid crystal module can be miniaturized by formation of the circumference circuit on a TFT substrate, and a high definition image can be offered.

[0084] [Example 2] Next, the 2nd example of this invention is explained. Drawing 22 is the block diagram of the liquid crystal display by the example 2. The point which is different from an example 1 is a part of signal side circumference circuit of a liquid crystal panel 11. Specifically, each terminal of the junction bus 19 is connected to the signal input selection circuitry 121 constituted from a shift register train through the level shifter 120.

[0085] The block diagram from the junction bus to the Rhine latch is shown in drawing 23 . A level shifter 120 is connected to the junction bus 19 connected to the chip output terminal 31 for every wiring, and a data electrical potential difference is changed into the logical level suitable for the logical circuit by TFT. The output of the level-shifter circuit 120 is inputted into the input terminal 109 of a shift register 122, respectively. It connects with a part for the number of stages equivalent to the block count which divides the data for one line, and a serial, and the shift register 122 constitutes the shift register train.

[0086] A shift register 122 operates with the shift clock 162 from the transfer control circuit 26. The shift clock 162 synchronizes with the memory chip block change signal 131 of a memory chip 12.

[0087] Drawing 24 is the explanatory view showing actuation of a signal input selection circuitry. The shift register train of the signal input selection circuitry 121 incorporates the data of each block inputted into the input terminal whenever the shift clock changed, and shifts them to the right one by one. If a shift action is repeatedly completed to block 1-h, the data of the k-th line will be sampled. If the Rhine latch control signal 132 is impressed at this time, the data for one line will be transmitted to the Rhine latch 23. Then, a display action is performed by the liquid crystal gradation drive circuit 24 like an example 1.

[0088] To having been required for the level shift circuit of an example 1 by one line, the level shift circuit of an example 2 can be managed with 1 block, and can reduce power consumption. The signal wiring of a 640x480-pixel panel will become 640 circuits if a level-shifter circuit is arranged after those with 640, and a selection latch circuit, but when it arranges after a signal input selection circuitry, only the number of the junction buses 19 is required, for example, if the number of junction buses is 40, it is good in 40 circuits and, specifically, the power consumption of this part can be cut down to 1/80.

[0089] Moreover, since the wiring intersection of a signal input selection circuitry can be decreased, increase of the power consumption by a logic electrical potential difference becoming high can be offset.

[0090] [Example 3] Drawing 25 shows the cross-section structure of the liquid crystal panel by other examples. The liquid crystal panel of a reflective mold is shown to the liquid crystal panel of the

transparency mold of drawing 4 . In this example, the reflective display electrode 141 is used as a display electrode, using a dichroic polymer dispersed liquid crystal or guest host mold liquid crystal as high reflective liquid crystal 140 used for a display.

[0091] The outline structure of a picture element part is shown in drawing 26 . The picture element part of a display 29 is an intersection of the shape of a matrix of the gate wiring 110 and the drain wiring 106, and consists of pixels TFT142 linked to these. The reflective mold display electrode 141 is formed with the metal thin film with a high reflection factor, and when the liquid crystal driver voltage impressed to the drain wiring 106 is inputted into a selection pulse by the gate wiring 110, it drives liquid crystal 140 by flowing through a drain electrode and the display electrode 141.

[0092] By using high reflective liquid crystal, a back light becomes unnecessary, and power consumption serves as only the image memory chip 12 and the TFT circumference circuit 40, and can perform much more reduction of power consumption.

[0093] [Example 4] Next, the example of the computing system which applied the liquid crystal display of this invention is explained. The example of the computing system by this invention is shown in drawing 27 . A keyboard 154 and a liquid crystal display 3 for this system to input CPU150 which carries out data processing of the information, the memory device 151 which memorizes data, I/O153 which controls data I/O with the system exterior, the controller 152 which performs control of a system, a command, etc. are mutually connected through the system bus 158. It is the configuration that an image memory chip is mounted in a liquid crystal panel, and it is only supplying the modification part and the indicative data from CPU150 can update the image display of a display as the liquid crystal display 3 was explained to the example 1 thru/or the example 3.

[0094] The liquid crystal display 3 of this system is connected to the independent display power source 157. System power 155 is a power source which drives except display 3, and has an electric power supply to each part controlled by CPU150 and the power control section 156 corresponding to the situation of a key input or a system bus 158. Usually, all components are worked and an input, an information operation, a display, etc. are performed. When restricted to a part of actuation, by CPU150, under count etc. can control system power, can intercept energization of an element [**** / un-], and can reduce power consumption.

[0095] Furthermore, when waiting for an input is carried out exceeding fixed time amount, system power 155 can be intercepted, CPU150 can be stopped, only a liquid crystal display 3 can be worked, and the screen display till then can be maintained. It can key from the condition and a system can also be rebooted.

[0096] Since the conventional liquid crystal display module always needs to supply an indicative data from CPU or a controller, if CPU or the controller of a computing system is stopped, the contents of a display will also disappear. However, since the image memory for the indicating equipment itself to hold an indicative data is built in according to the computer system of this example, when there is no need for operation of other equipments of a system, even if it intercepts the electric power supply, a display action can be maintained, and it is effective in the ability to reduce the power consumption of a system sharply.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The basic block diagram of the liquid crystal display of this invention.
[Drawing 2] The outline block diagram of the conventional TFT-liquid-crystal display module.
[Drawing 3] The block diagram of the liquid crystal display by the example 1 of this invention.
[Drawing 4] The fragmentary sectional view of the liquid crystal display of an example 1.
[Drawing 5] The block diagram of an image memory.
[Drawing 6] The circuit diagram of a memory cell.
[Drawing 7] The circuit diagram of a sense amplifier.
[Drawing 8] Memory output latch's block diagram.
[Drawing 9] Memory output latch's circuit diagram.
[Drawing 10] Latch selection-circuitry Fig.
[Drawing 11] Block electronic switch Fig.
[Drawing 12] The block diagram of the selection latch circuit of TFT, and the Rhine latch circuit.
[Drawing 13] The circuit diagram of a level shifter.
[Drawing 14] Liquid crystal gradation drive circuit diagram.
[Drawing 15] A shift register and a gate drive circuit diagram.
[Drawing 16] Shift register circuit diagram.
[Drawing 17] The timing diagram which shows the data write-in procedure of an image memory.
[Drawing 18] The timing diagram which shows latch actuation of an image memory output.
[Drawing 19] The explanatory view of the selection actuation outputted to a junction bus from an image memory chip.
[Drawing 20] The explanatory view of selection actuation inputted into a signal side circumference circuit from a junction bus.
[Drawing 21] The timing diagram which shows TFT Rhine latch actuation.
[Drawing 22] The block diagram of the liquid crystal display by the example 2 of this invention.
[Drawing 23] The block diagram of the signal side circumference circuit by the example 2.
[Drawing 24] The explanatory view showing the data array of a shift register train.
[Drawing 25] The fragmentary sectional view of the liquid crystal display of an example 3.
[Drawing 26] The outline block diagram of a picture element part.
[Drawing 27] The block diagram of the computing system by the example 4 of this invention.
[Description of Notations]
1 [-- Rhine memory parallel interface,] -- A data address bus, 2 -- A control signal line, 3 -- A display, 4 5 -- A connection, 6 -- A parallel input interface, 7 -- Liquid crystal gradation drive circuit, 8 -- Serial transmission data, 9 -- A serial parallel conversion circuit, 11 -- Liquid crystal display panel, 12 -- An image memory chip, 13 -- An image memory, 14 -- Data-line decoder, 15 -- Word line DEKOTA, 16 -- A memory output latch, 17 -- Latch selection circuitry, 18 -- A read-out control circuit, 19 -- A junction bus, 20 -- Block electronic switch, 21 -- A selection latch circuit, 22 -- A level shifter, 23 -- Rhine latch, 24 -- A liquid crystal driver voltage generating circuit, 26 -- A transfer control circuit, 27 -- Gate wiring

drive circuit, 28 [-- Chip output connection terminal,] -- A shift register, 29 -- A display, 30 -- CPU, 31 32 -- A signal side circumference circuit, 33 -- A scan side circumference circuit, 34 -- Address bus wiring, 35 -- Data bus wiring, 37 -- A chip input connection terminal, 38 -- Bus wiring, 40 [-- Liquid crystal,] -- A TFT circumference circuit, 41 -- A TFT substrate, 42 -- An opposite substrate, 43 44 [-- Gradation power source,] -- A liquid crystal seal, 45 -- A polarizing plate, 46 -- A back light, 47 49 -- The transparence electric conduction film, 48 -- A color filter, 50 -- Data interface, 51 [-- Sense amplifier,] -- A bit line drive circuit, 62 -- A word line, 63 -- A memory cell, 64 65 [-- Reversal bit terminal,] -- A bit line, 68 -- A WORD terminal, 69 -- A bit terminal, 70 71 -- A bit line input terminal, 72 -- Data output, 81 -- Output block, 82 -- An output bus, 83 -- A block analog switch, 84 -- Block selection signal, 85 [-- Block latch signal,] -- An inverter, 86 -- An input bus, 87 -- A block output, 88 89 -- An inverter, 90 -- An inverter circuit, 91 -- Transfer gate circuit, 92 [-- Power supply terminal,] -- A control inverter, 93 -- An input terminal, 97 -- A latch circuit, 99 100 -- An input terminal, 101 -- A DEKOTA circuit, 103 -- Transfer gate, 104 -- A gradation voltage selection switch, 105 -- A gradation electrical-potential-difference bus, 106 -- Output line (drain wiring), 107 -- An inverter, 108 -- The transfer gate, 110 -- Gate wiring, 111 -- An inverter train, 112 -- A shift register, 113 -- Shift clock circuit, 114 -- A frame start signal, 120 -- A level shifter, 121 -- Signal input selection circuitry (shift register train), 122 -- A shift register, 130 -- Memory chip block change signal, 131 -- A memory latch control signal, 132 -- The Rhine latch signal, 135 -- Analog switch, 140 -- High reflective liquid crystal, 141 -- A reflective display electrode, 142 -- Pixel TFT, 150 [-- I/O,] -- CPU, 151 -- Memory, 152 -- A controller, 153 154 [-- A display power source, 158 / -- A system bus, 160 / -- A TFT block analog switch, 161 / -- TFT analog switch.] -- A keyboard, 155 -- System power, 156 -- The power control section, 157

[Translation done.]

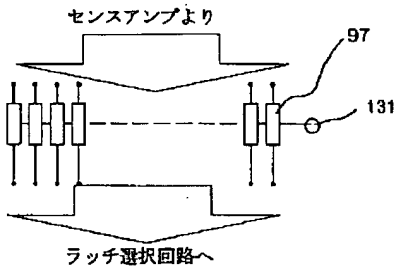
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

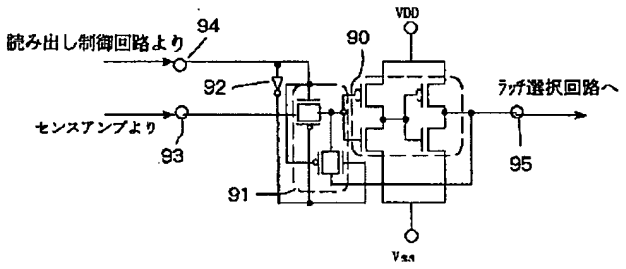
[Drawing 8]

図 8



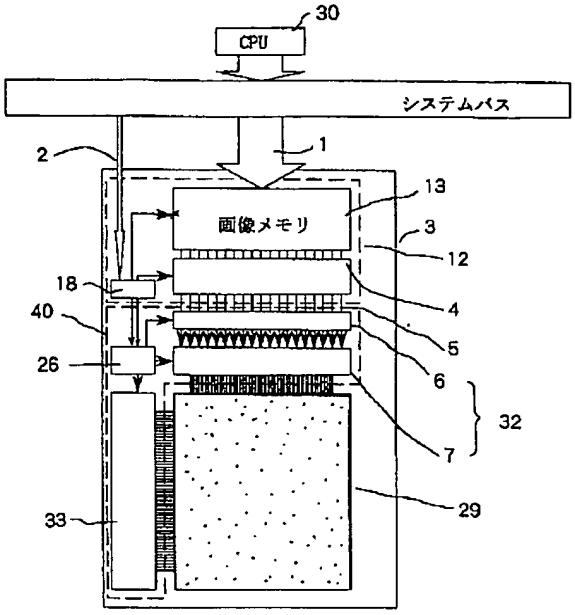
[Drawing 9]

図 9



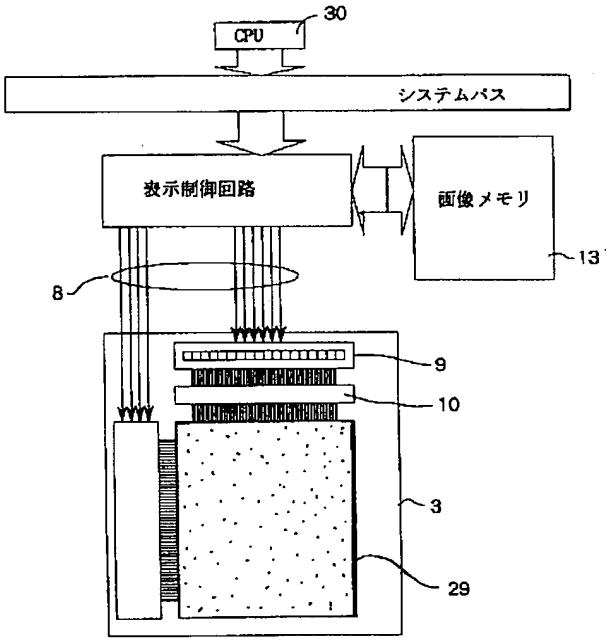
[Drawing 1]

図 1



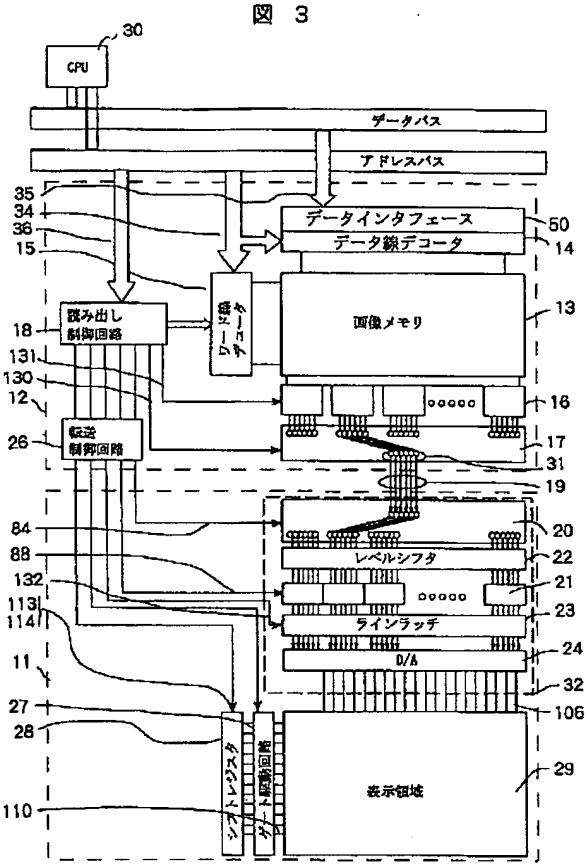
[Drawing 2]

図 2



[Drawing 3]

図 3



[Drawing 4]

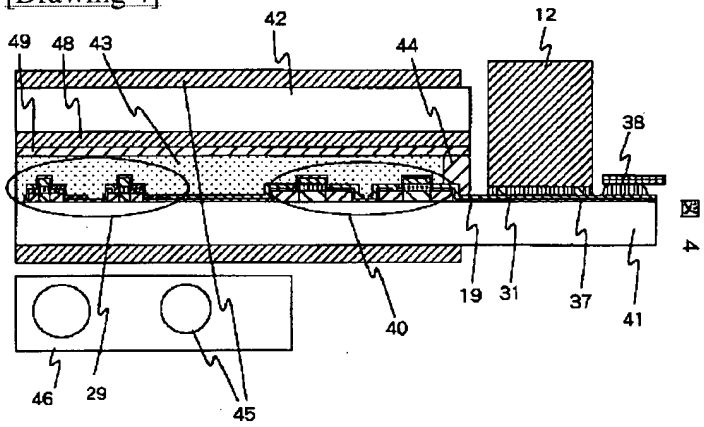
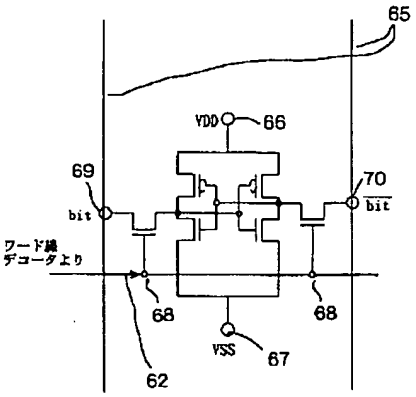


図 4

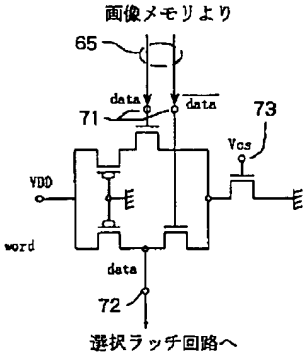
[Drawing 6]

図 6



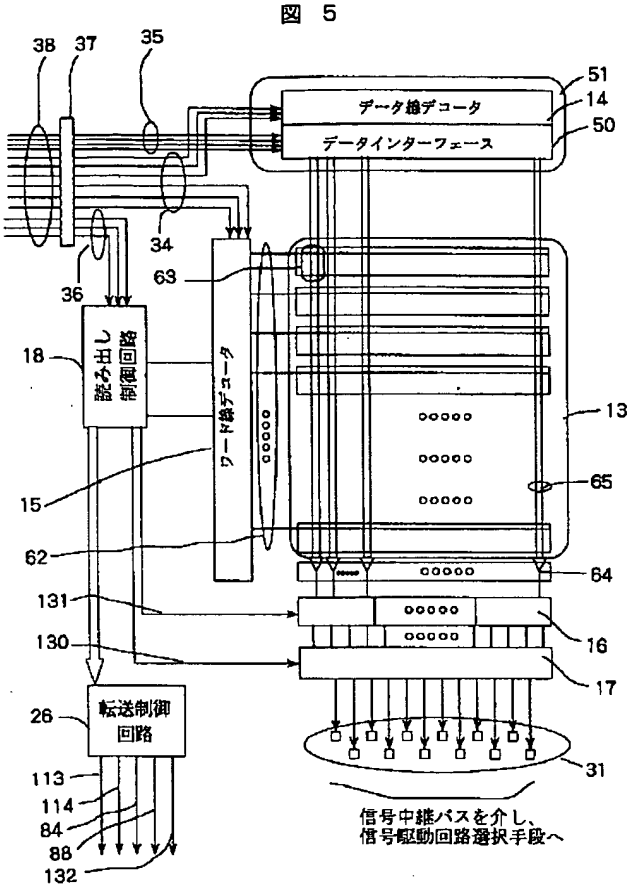
[Drawing 7]

図 7



[Drawing 5]

図 5



[Drawing 10]

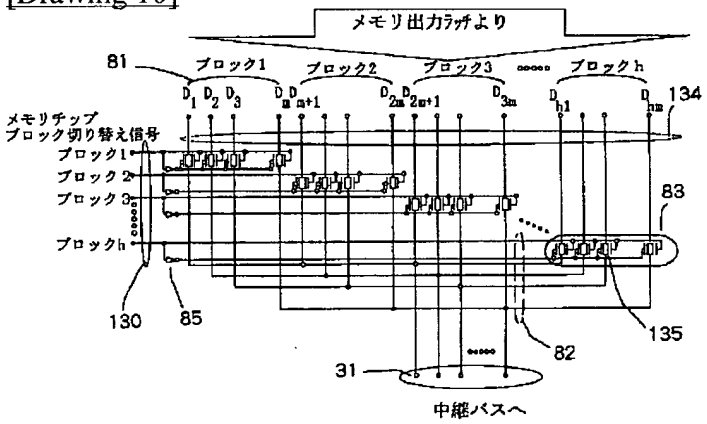
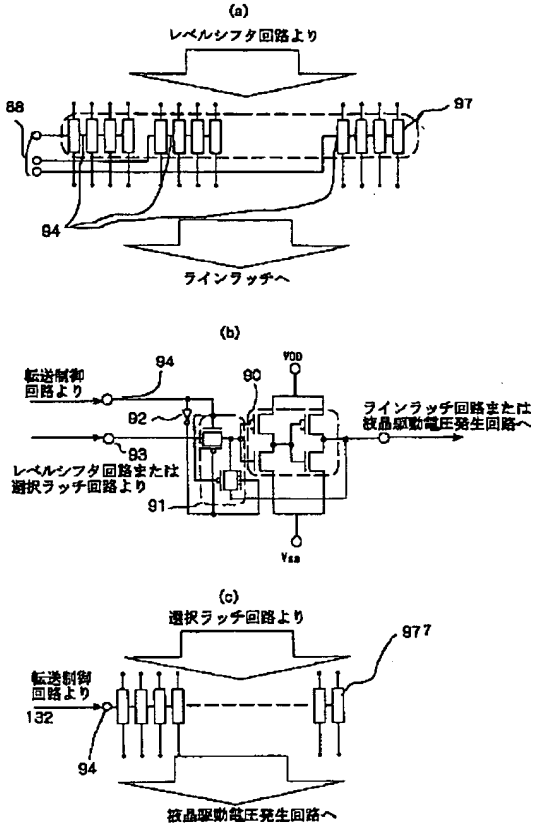


図 10

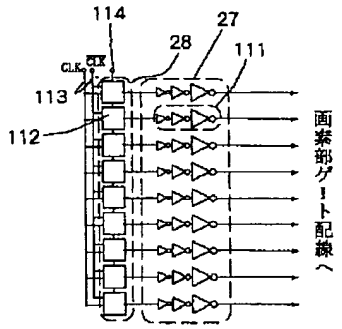
[Drawing 12]

図 12



[Drawing 15]

図 15



[Drawing 17]

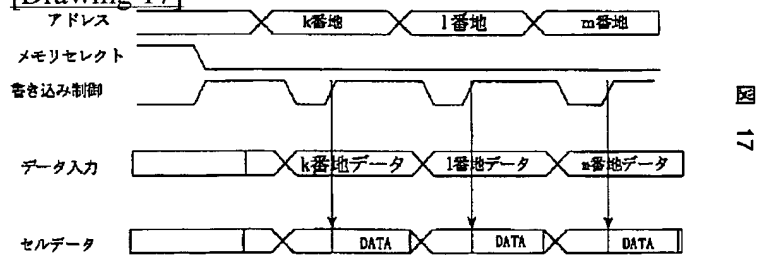


図 17

[Drawing 11]

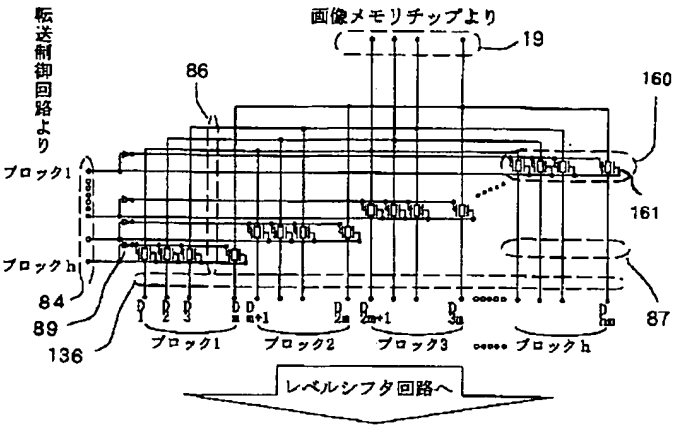
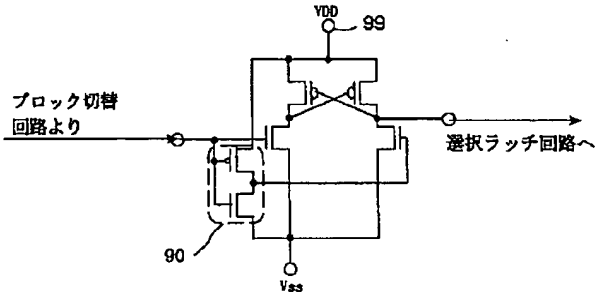


図 11

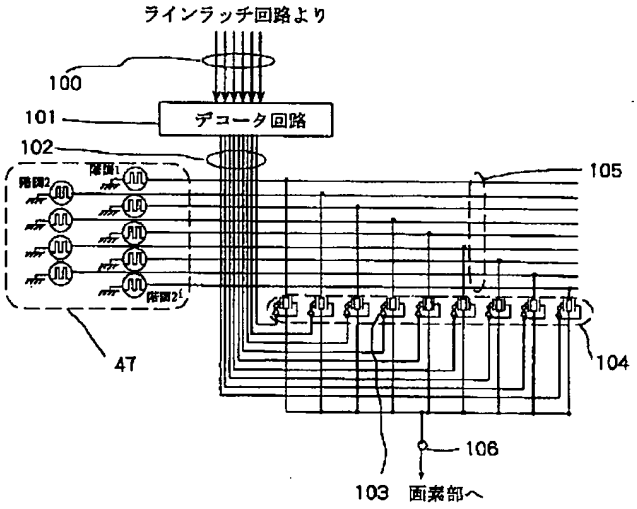
[Drawing 13]

図 13



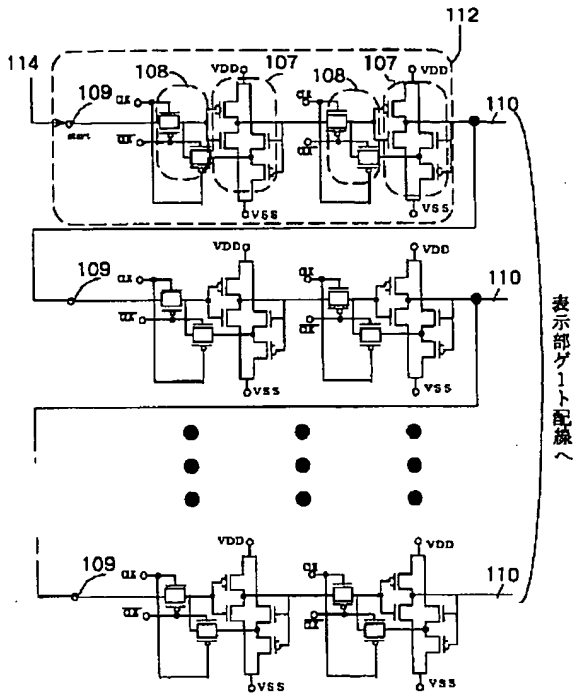
[Drawing 14]

図 14



[Drawing 16]

図 16



[Drawing 18]

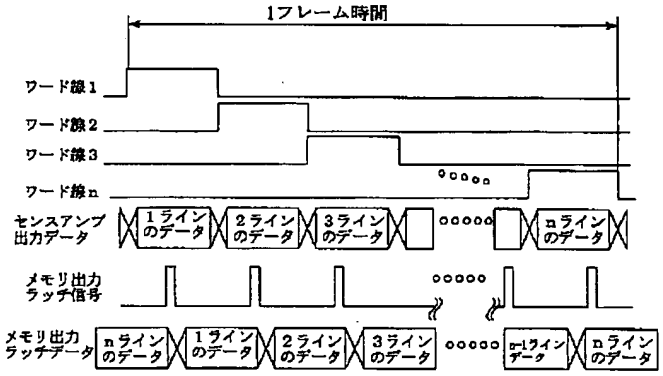
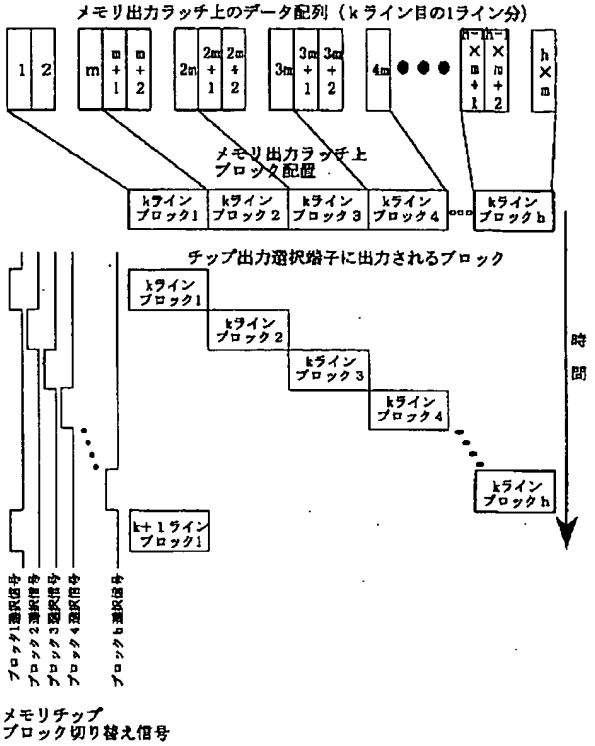


図 18

[Drawing 19]

図 19



[Drawing 20]

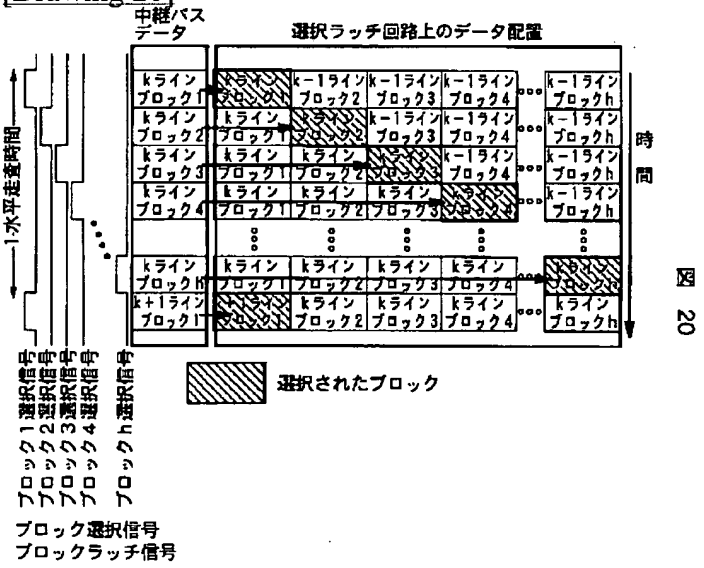


図 20

[Drawing 21]

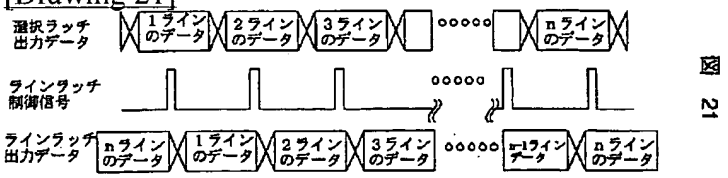
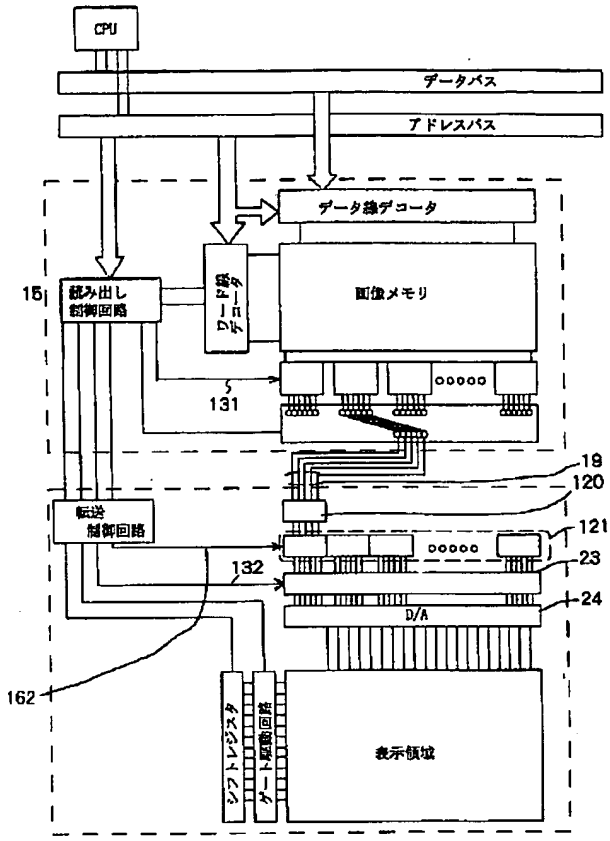


図 21

[Drawing 22]

図 22



[Drawing 24]

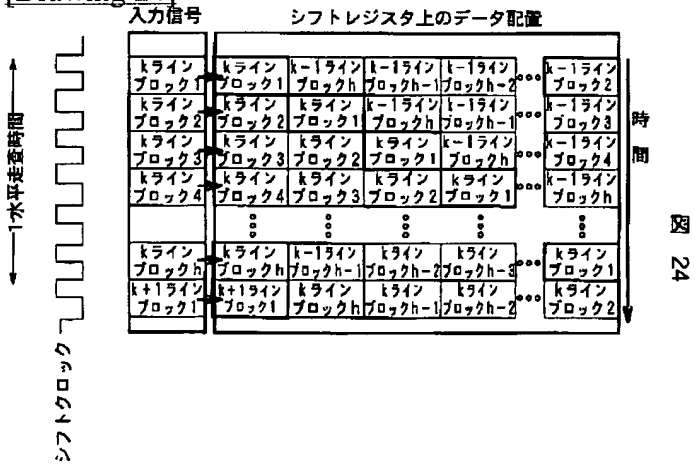
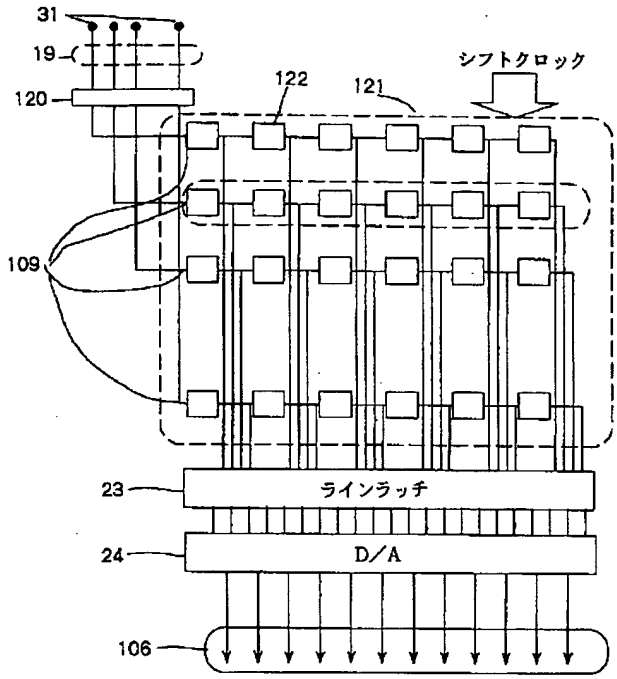


図 24

[Drawing 23]

図 23



[Drawing 25]

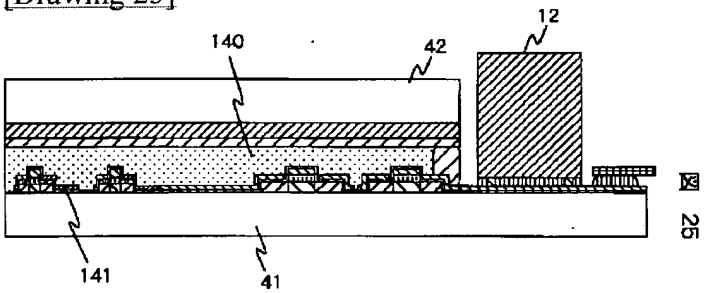
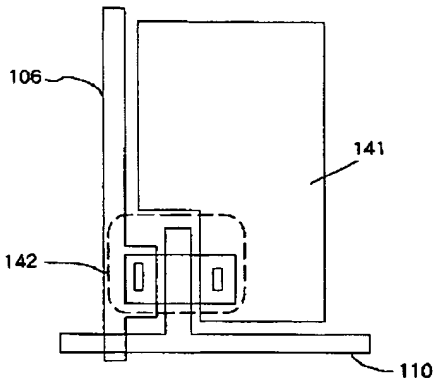


図 25

[Drawing 26]

図 26



[Drawing 27]

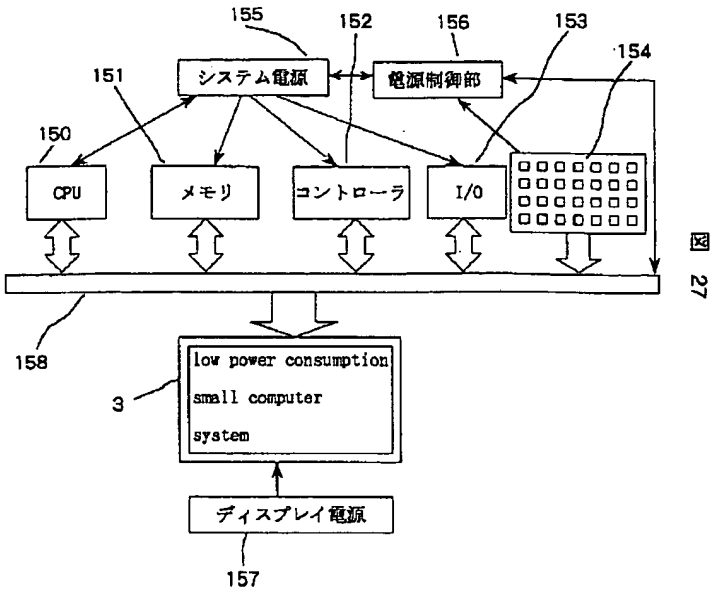


図 27

[Translation done.]

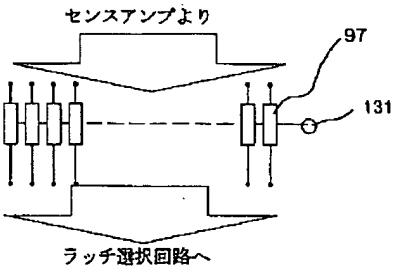
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

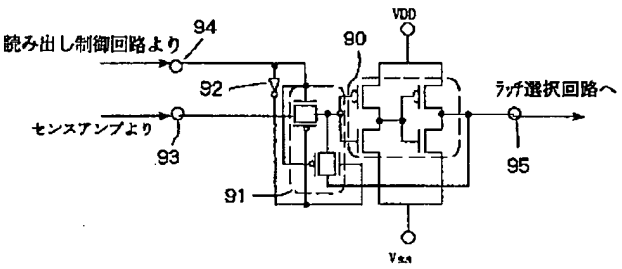
[Drawing 8]

図 8



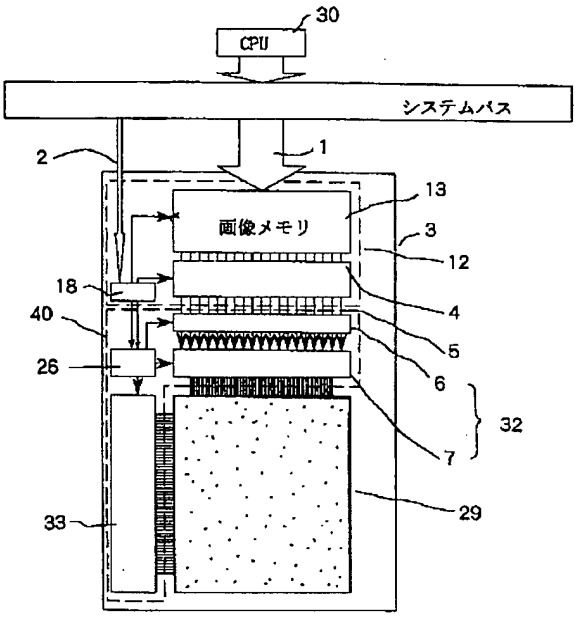
[Drawing 9]

図 9



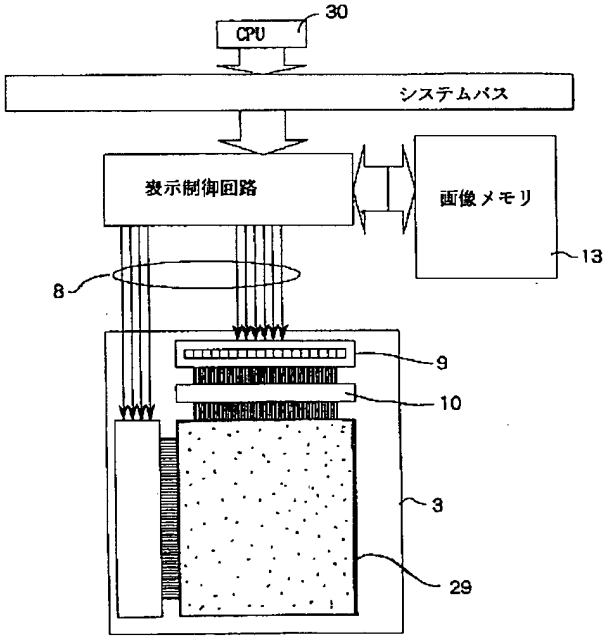
[Drawing 1]

図 1



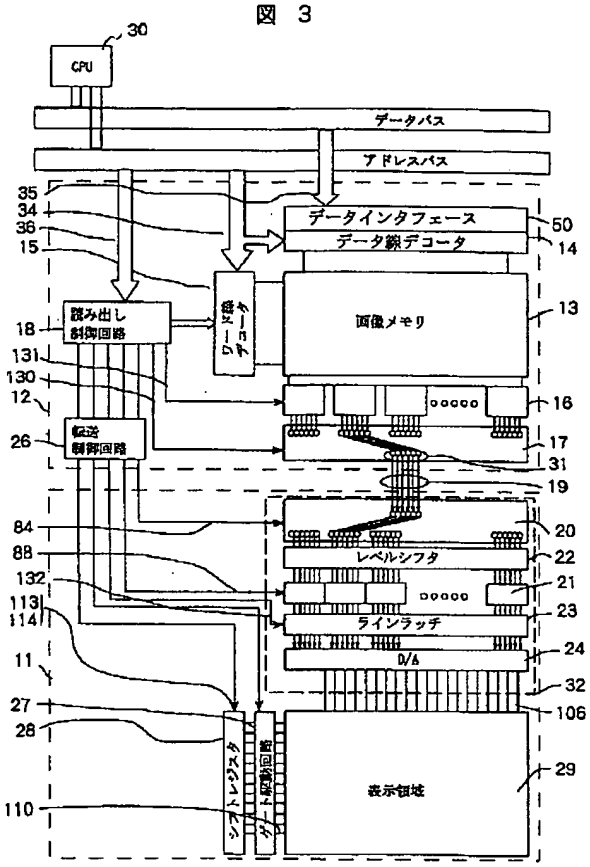
[Drawing 2]

図 2



[Drawing 3]

図 3



[Drawing 4]

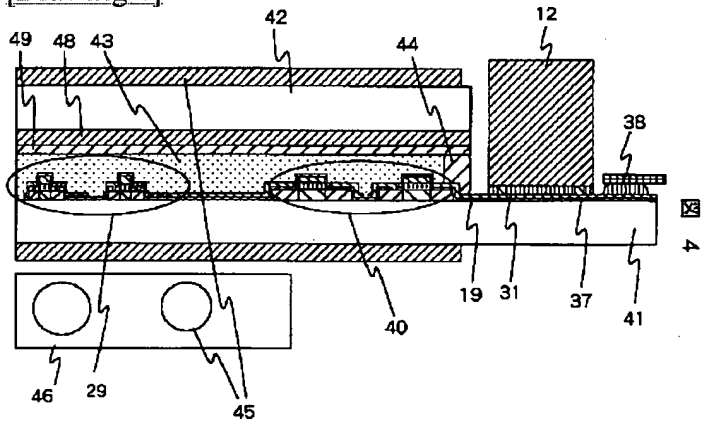
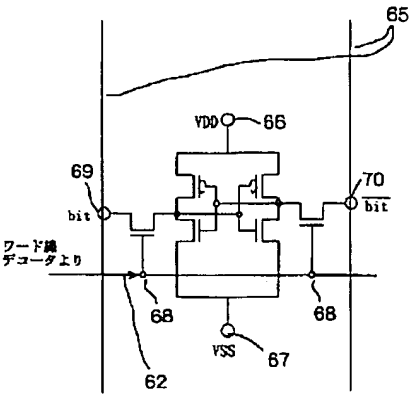


図 4

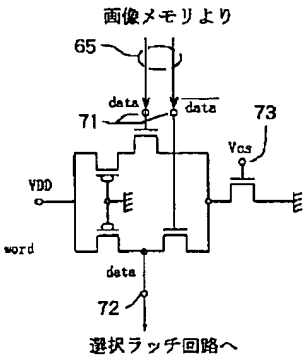
[Drawing 6]

図 6



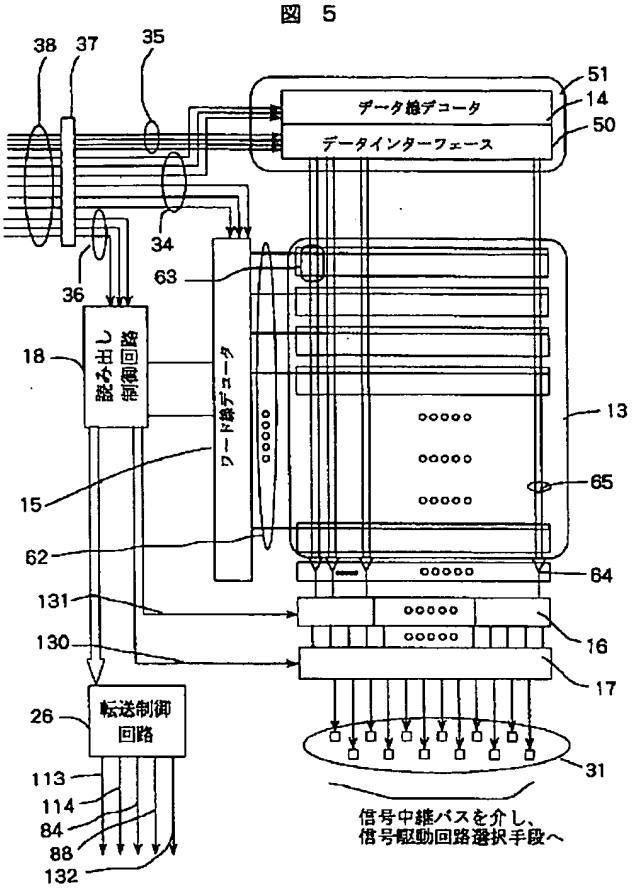
[Drawing 7]

図 7



[Drawing 5]

図 5



[Drawing 10]

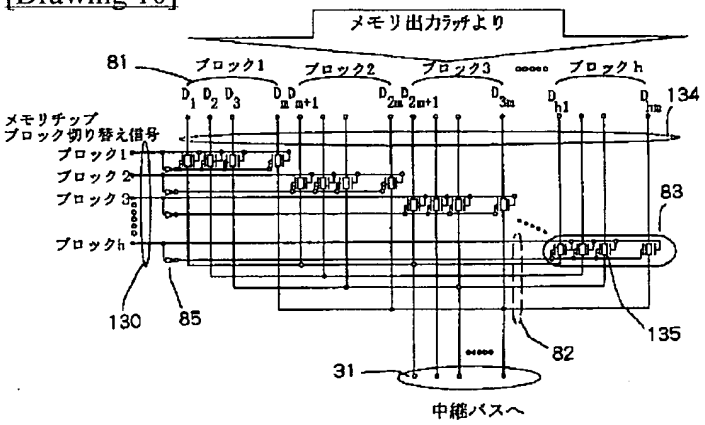
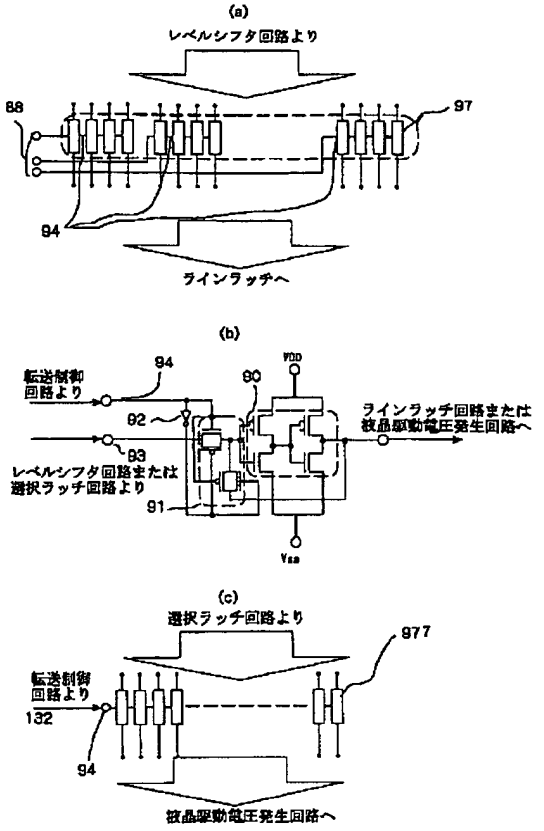


図 10

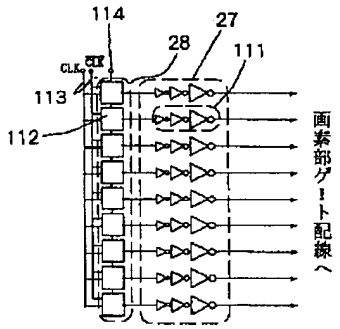
[Drawing 12]

図 12



[Drawing 15]

図 15



[Drawing 17]

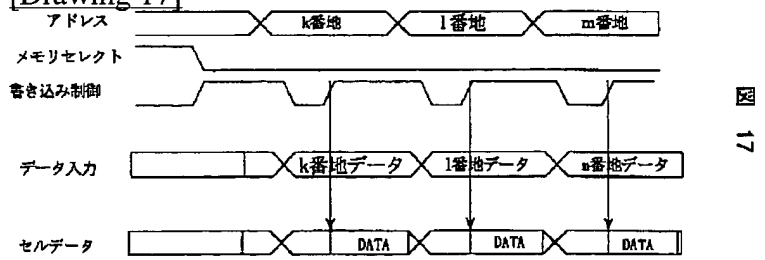


図 17

[Drawing 11]

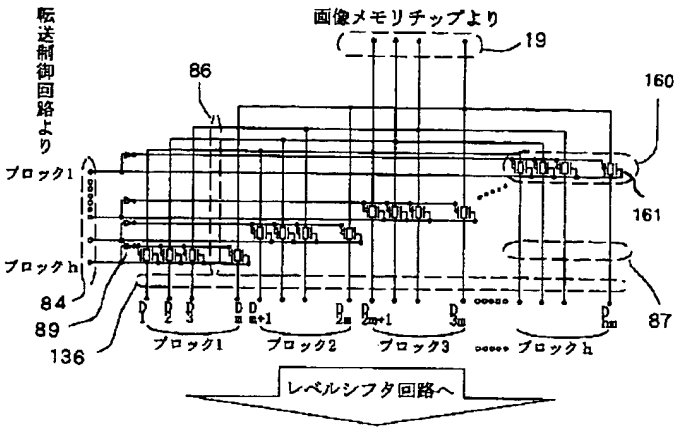
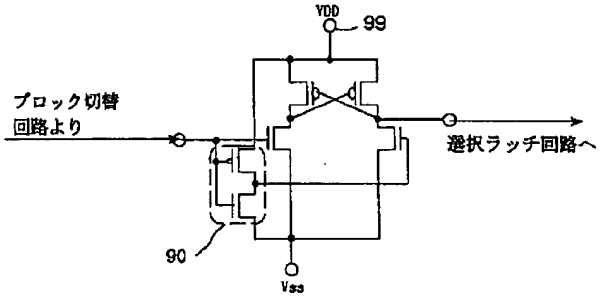


図 11

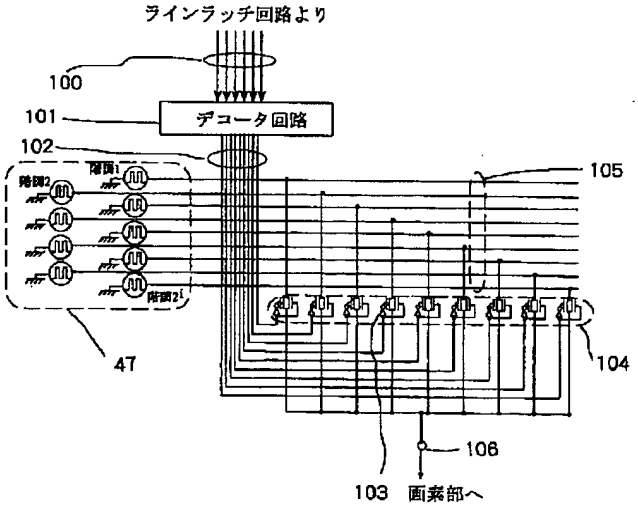
[Drawing 13]

図 13



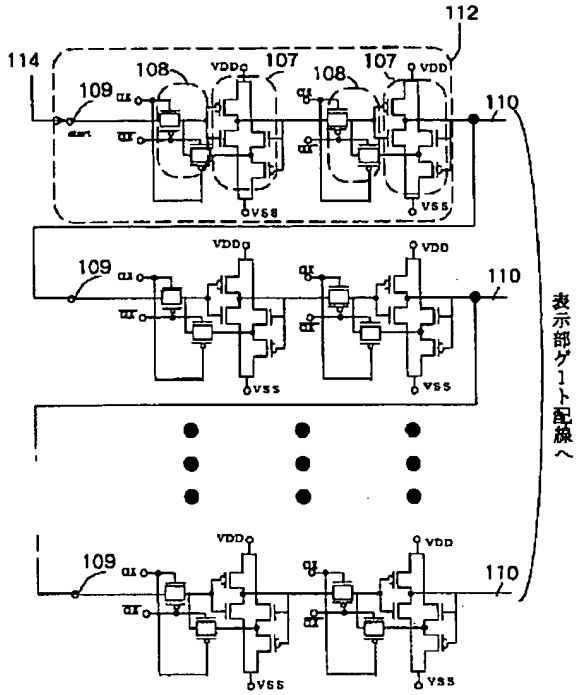
[Drawing 14]

図 14



[Drawing 16]

図 16



[Drawing 18]

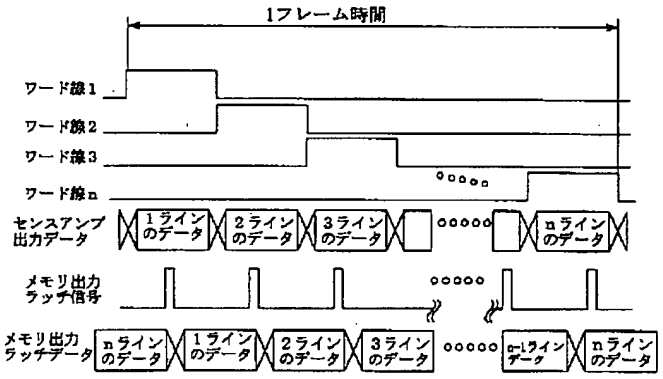
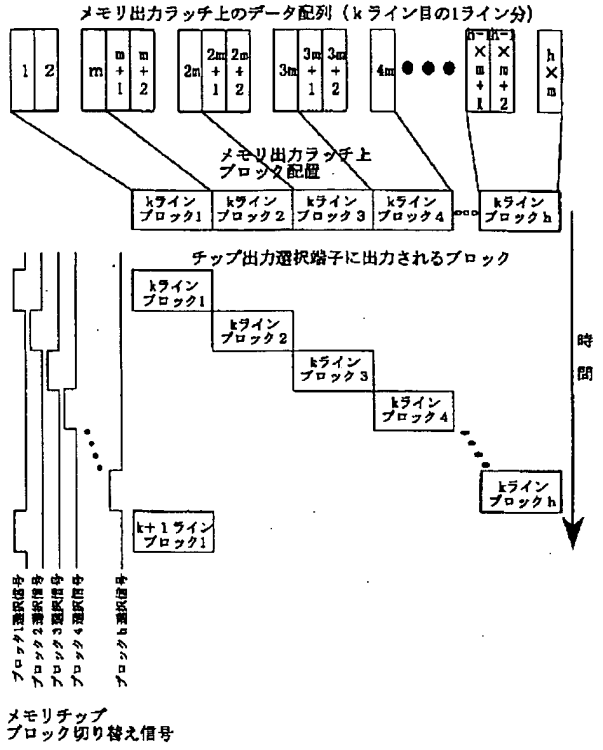


図 18

[Drawing 19]

図 19



[Drawing 20]

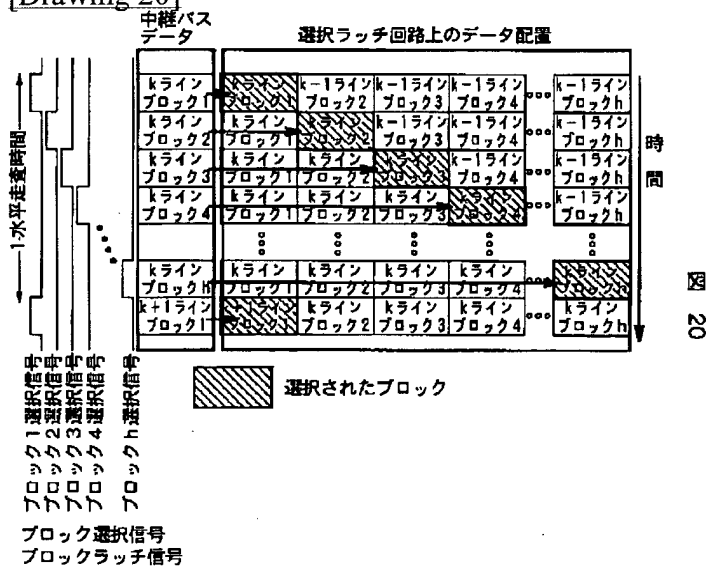


図 20

[Drawing 21]

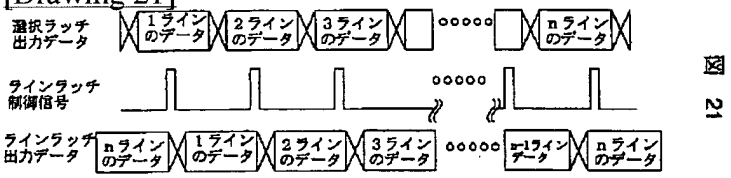
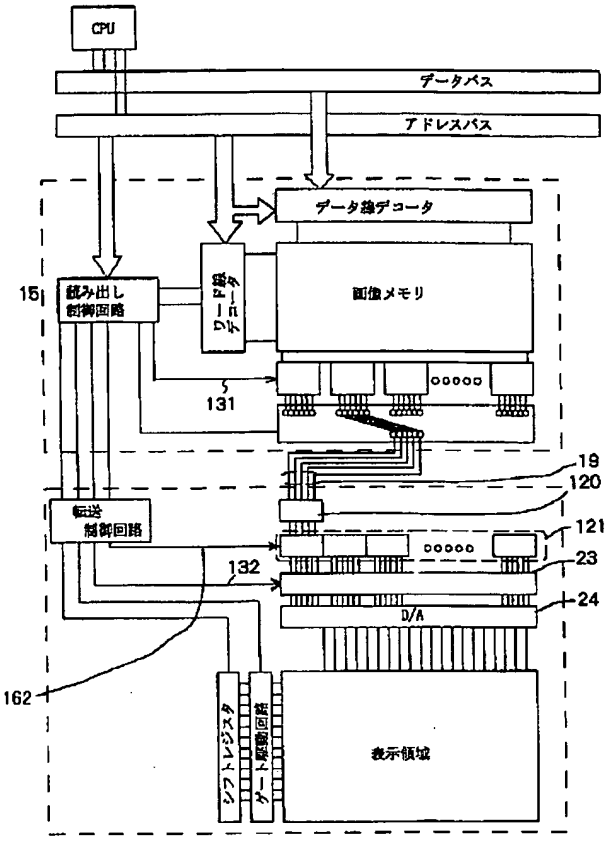


図 21

[Drawing 22]

図 22



[Drawing 24]

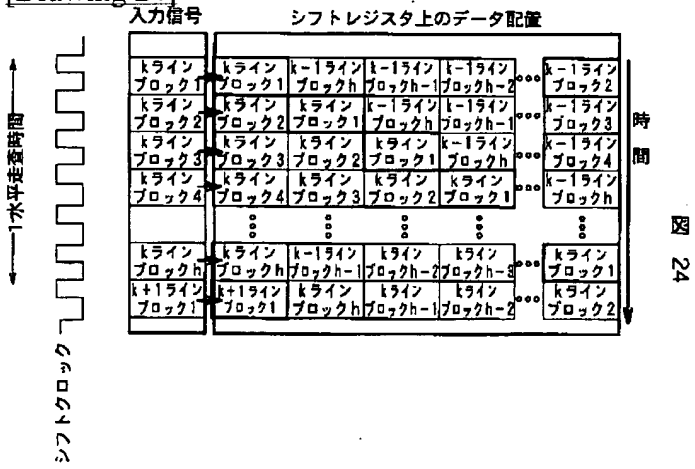
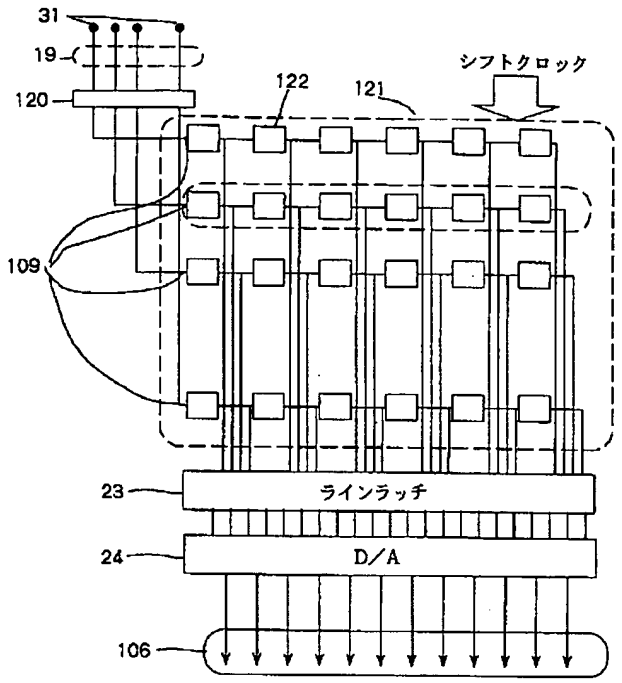


図 24

[Drawing 23]

図 23



[Drawing 25]

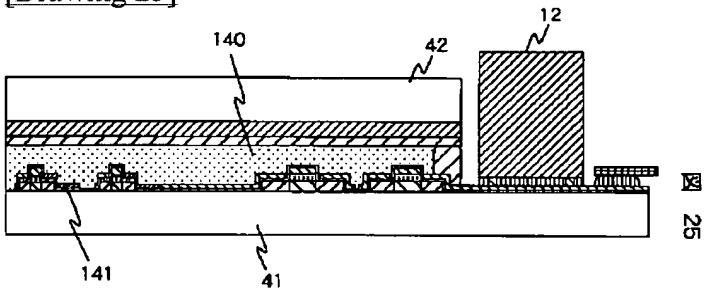
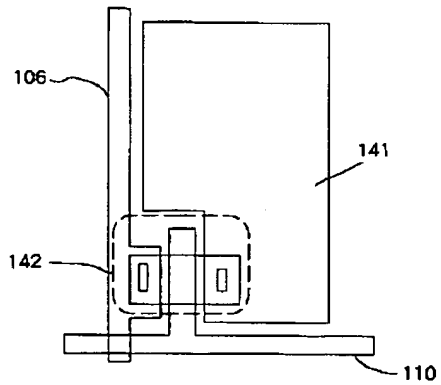


図 25

[Drawing 26]

図 26



[Drawing 27]

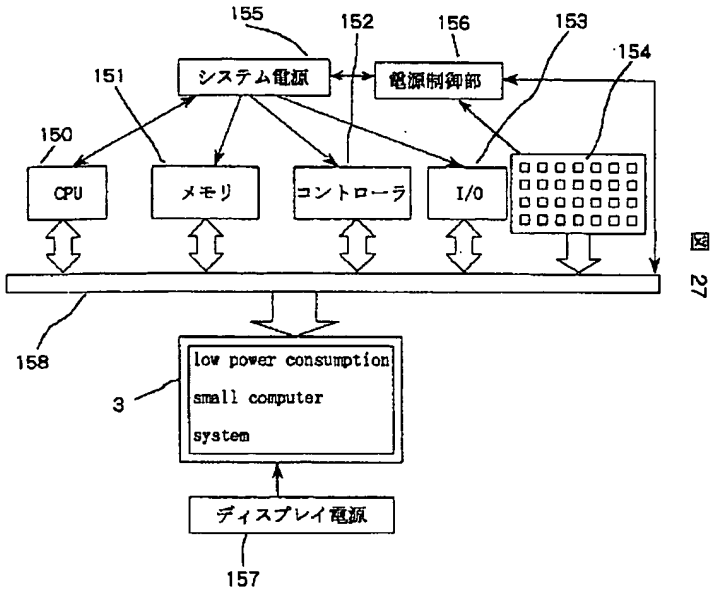


図 27

[Translation done.]